Part Number M6775
Rev. B

# ModulasTen M68K10
# 68000 MULTIBUS Single-Board Computer
# Reference Manual

This manual applies to M68K10 boards with serial numbers 0 through 3328 and 3331 through 3727, inclusive.

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF JUMPER AREAS

The following list shows the function of each jumper area, its location on the M68K10 board, and the main section(s) in this manual where the jumper area is discussed. Most of the jumper locations are given in relation to the sockets on the M68K10 (e.g., "below U42," etc.). The board's sockets are (roughly) numbered from left to right in rows across the board.

See section 3-3 for a list of the standard jumperings of the M68K10.

| Jumper Area | Function | Location On M68K10 | Section Of Manual |
|---|---|---|---|
| J1 | 50-pin serial I/O header connector | top left of board | 5-1 |
| J2 | 50-pin I/O header connector | top rt. of board | 5-2 |
| J3 | Reset connector | left of switch S1 (top of board) | 5-4 |
| J4 | access time for PROM and for dynamic RAM | between U45 & U46 | 3-4-2; 3-5-2 |
| J5 | enable/disable bus error timeout on MULTIBUS accesses | below U15 | 3-11 |
| J6 | (with J29) - enable on-board interrupts and MULTIBUS interrupts | below U66 (bottom of board) | 3-10 |
| J7 | select on-board or external clock source | below U45 | 3-8-1 |
| J8 | select on-board timer clock frequency | above U46 | 3-7 |
| J10 | select on-board slave memory address | below U65 (bottom of board) | 3-8-5 |
| J11 | select MULTIBUS slave memory address | right of U64 | 3-8-5 |
| J13 | connect BPRO signal to MULTIBUS | below U29 | 3-8-2 |
| J14 | connect INIT signal to MULTIBUS | below U42 | 3-8-3 |
| J15 | connect BCLK signal to MULTIBUS | below U62 (bottom of board) | 3-8-1 |
| J16 | connect CCLK signal to MULTIBUS | right of C2 (bottom of board) | 3-8-1 |
| J17 | (with J18) - amount of memory on MXM10 | above U39 | 3-5-1 |
| J18 | (with J17) - amount of memory on MXM10 | right of U32 | 3-5-1 |

(continued on next page)

LIST OF JUMPER AREAS

| Jumper Area | Function | Location On M68K10 | Section Of Manual |
|---|---|---|---|
| J19 | clock rates and RAM speeds | right of U21 | 3-5-3 |
| J20 | connector for MXM10 module | right of U74 | 3-5-1 |
| J21 | size of memory components in 28-pin sockets; RAM option for U5 & U35 | below U6 | 3-4-1; 3-4-6 |
| J22 | type of memory component in socket U17 | right of U17 | 3-4-3 |
| J23 | type of memory component in socket U35 | right of U35 | 3-4-3 |
| J24 | type of memory component in socket U16 | right of U16 | 3-4-3 |
| J25 | type of memory component in socket U5 | right of U5 | 3-4-3 |
| J26 | source of power for 28-pin PROM sockets | below J2 conn. | 3-4-5 |
| J27 | baud rates for channels A and B | right of U10 | 3-6 |
| J28 | select between J27-jumpered baud rate and programmable baud rate for ch. A & B | above U9 | 3-6 |
| J29 | (with J6) - enable on-board interrupts and MULTIBUS interrupts | below J31 (iSBX connector) | 3-10 |
| J30 | extension of J31 connector pins 28 & 30 | left of J31 | 5-5-1 |
| J31 | iSBX module connector | below U15 | 5-5 |
| J32 | extension of J33 connector pins 28 & 30 | below J33 | 5-5-1 |
| J33 | iSBX module connector | below U19 | 5-5 |
| J34 | (with J35) - parallel & timer I/O options | below J2 conn. | 3-7 |
| J35 | (with J34) - parallel & timer I/O options | below J2 conn. | 3-7 |
| J36 | connect BPRN input to MULTIBUS or Ground | above U43 | 3-8-2 |
| J37 | connect CBRQ input to MULTIBUS or Ground | below U28 | 3-8-2; 3-8-4 |
| J40 | battery backup connector | above U5 (top of board) | 5-3 |

ModulasTen™ M68K10™

68000 MULTIBUS* SINGLE-BOARD COMPUTER

REFERENCE MANUAL

## 1. PRODUCT DESCRIPTION

The M68K10™ is a high-performance MULTIBUS*-compatible single-board computer featuring a 10 MHz 68000 microprocessor. It is designed to function as a stand-alone microcomputer, a single CPU/controller in a MULTIBUS system, or a single CPU element in a multiprocessor configuration. The M68K10 allows users to take advantage of the wide choice of I/O and memory products compatible with the MULTIBUS and iSBX* standards, and to enjoy the superior performance and ease of programming provided by the 68000 family of microprocessors.

The 68000's 32-bit internal architecture, speed, and well-designed instruction set account for its high popularity among OEMs who are building systems that must perform sophisticated tasks. For systems which must respond to real-time events, or systems in which execution speed is critical, the 68000's superior assembly language instruction set is highly advantageous.

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## 1-1 Memory

Dual-Ported Dynamic RAM. The M68K10 can be configured with up to 256K bytes of fast on-board dynamic RAM using 64K by 1 bit memory components. A simple jumper change allows the M68K10 to accommodate 256K by 1 bit memory components, increasing the on-board dynamic RAM capacity to one Megabyte.

One half of the M68K10´s dynamic RAM is resident on-board; the remainder is provided by the MXM10 memory expansion module. With 64K-byte memory components, the M68K10 can supply 128K bytes of dynamic RAM without an MXM10. The MXM10 expansion module is required only if your application requires more than 128K bytes of memory.

The 68000 operates at full speed when accessing on-board dynamic RAM; an on-board memory read or write operation requires only 400 nanoseconds. The M68K10 automatically performs the periodic refresh operation required to maintain the data stored in dynamic RAM. The refresh controller interleaves the refresh operations with normal data accesses.

Part or all of the M68K10´s on-board dynamic RAM may be accessed by other MULTIBUS masters just as if the M68K10 were a memory board. Jumpers allow this dual-ported RAM to be addressed on any 64K byte boundary within the MULTIBUS´s 16 Megabyte address space.

EPROM And Static RAM. Two pairs of 28-pin sockets on the M68K10 accept a wide variety of EPROMs and RAMs. The first pair of sockets is used for up to 32K bytes of EPROM-resident code, which must include a small power-up bootstrap program. PROBUG (tm), the interactive debugger/monitor often used with the M68K10, contains the required bootstrap.

The second pair of sockets can be used either for additional EPROMs or for static RAMs. A total of 64K bytes of EPROM can be accommodated; alternatively, 32K bytes of EPROM can be combined with 16K bytes of static RAM. CMOS static RAM can be powered by external batteries, and can be write-protected in case the main power supply is turned off. On-board jumpers allow selection of memory component size and the battery back-up option.

## 1-2 Input/Output

The input/output (I/O) capabilities of the M68K10 include two RS-232C-compatible serial channels, twenty-four bits of parallel I/O, three 16-bit counter/timers, and eight software-controllable status LEDs. Two independent iSBX connectors allow you to add extra I/O to a system without adding MULTIBUS I/O boards.

The two RS-232C serial channels are implemented with a Multi-Protocol Serial Controller (MPSC). In addition to standard asynchronous formats, the MPSC also supports IBM Bisync and SDLC formats. A dual baud rate generator may be used to select one of 16 standard rates for each channel. Alternatively, one or both channels may be set up for a programmable baud rate generated by one of the counter/timers. The MPSC will operate at rates up to 880K baud.

Channel A includes all the handshake signals required by terminals, printers, and modems. Channel B does not require the handshake signals, and does not support these signals. A 50-pin connector at the top of the board is wired so that two 25-pin D-type connectors may be directly connected via flat-cable.

The 24 parallel I/O lines are divided into three 8-bit ports: port A, port B, and port C. All 8 bits of port A or B are programmed as a group for either input or output; also port A may be programmed as a bi-directional I/O bus. The 8 bits of port C may be programmed in groups of 4 bits as either input or output; or some of them may be programmed as handshake lines for ports A and B.

The triple counter/timer can be configured to generate a programmable baud rate, time-of-day clock interrupt, external timing signals, etc. Eight programmable LEDs provide a simple operator interface for indicating board or system status.

Each of the two iSBX connectors on the M68K10 supports an industry-standard I/O expansion interface. Numerous manufacturers provide I/O modules compatible with this interface. These modules may be used to expand parallel and serial I/O, or to add I/O functions such as an IEEE-488 interface, Bubble Memory, a SASI* disk interface, time-of-day clock/calendar, or analog I/O.

## 1-3 MULTIBUS Interface

The M68K10's MULTIBUS interface supports operation in a multi-master environment. Either daisy-chained serial or parallel bus arbitration may be selected. All 24 address lines of the 68000 are brought out to the MULTIBUS.

128K bytes of the 68000's total address space is used for on-board I/O (64K bytes) and static RAM/EPROM (64K bytes). Additionally, the M68K10 can have up to 1 Megabyte of dynamic RAM. This leaves at least 14.75 Megabytes of accessible MULTIBUS memory. Since on-board I/O does not occupy any of the MULTIBUS's 64K byte I/O range, the full 64K bytes is available.

The 68000 stores the two bytes within a 16-bit word in the opposite order from the MULTIBUS standard. To compensate for this, the M68K10 automatically swaps bytes when doing word accesses to or from MULTIBUS memory. On byte accesses, it also reverses the meaning of the low-order address bit so that bytes as well as words are accessed correctly. The byte swap logic also functions for slave accesses, delivering data in the order that the MULTIBUS requires.

## 1-4 Interrupts

The M68K10 supports seven levels of automatically vectored interrupts. Six of these levels may be driven by either on-board sources or the interrupt request pins of the MULTIBUS; or externally via the J2 connector. The remaining seventh level is non-maskable and is driven by pushbutton switch S1, located in the upper right-hand corner of the M68K10 board.

## 1-5 On-Board Addressing

The M68K10's on-board dynamic RAM begins at address $000000, so MULTIBUS memory cannot begin until after the location at which on-board RAM ends. For example, with 256K bytes of on-board dynamic RAM, the first memory location accessible on the MULTIBUS is $40000.

MULTIBUS memory extends from the end of on-board memory to location $FBFFFF. The 28-pin sockets occupy the range between $FC0000 and $FCFFFF. On-board I/O occupies the range between $FD0000 and $FDFFFF, and MULTIBUS I/O begins at $FE0000. Address $FF0000 up is unused.

# 2. M68K10 SPECIFICATIONS

## 2-1 CPU

10 MHz 68000

CPU clock and MULTIBUS clocks CCLK and BCLK: 10.0 MHz ±0.01%

Cycle Time: Basic instruction cycle = 400 ns

## 2-2 Memory

Memory Cycle Time (on-board)

RAM - 400 ns
EPROM - 500 to 800 ns (jumper-selectable)

Memory Capacity/Addressing

| EPROM/device | Total Capacity | Address Range |
|---|---|---|
| 2K bytes | 8K bytes | $FC0000 - $FC1FFF |
| 4K bytes | 16K bytes | $FC0000 - $FC3FFF |
| 8K bytes | 32K bytes | $FC0000 - $FC7FFF |
| 16K bytes | 64K bytes | $FC0000 - $FCFFFF |

| RAM (64K devices) | Total Capacity | Address Range |
|---|---|---|
| Without MXM10 | 128K bytes | $000000 - $01FFFF |
| With MXM10 | 256K bytes | $000000 - $03FFFF |

## 2-3 Input/Output

Serial - Two multiprotocol channels using one 8274 MPSC or equivalent.

Parallel - 24 programmable lines using one 8255A-5 Programmable Peripheral Interface (PPI) or equivalent.

Counter/Timer - Three 16-bit BCD or binary event counter/timers using one 8253-5 counter/timer or equivalent.

MULTIMODULE* - Two iSBX connectors compatible with byte-wide MULTIMODULEs.

LED - Eight software-controllable status LEDs.

## 2-4 Serial Communications

Two independent full duplex transmit/receive channels, with RS-232C drivers and receivers.

Asynchronous Operation:

- -5 to 8 bit character; odd, even, or no parity; 1, 1.5 or 2 stop bits
- -Error detection: framing, overrun and parity

Byte Synchronous Operation:

- -Character synchronization, internal or external
- -One or two sync characters
- -Automatic CRC generation and checking (CRC-16)
- -IBM Bisync compatible

Bit Synchronous Operation:

- -SDLC/HDLC flag generation and recognition
- -8-bit address recognition
- -Automatic zero bit insertion and deletion
- -Automatic CRC generation and checking (CCITT-16)
- -CCITT X.25 compatible

Baud Rates - 3 options, independently selectable for each channel:

-Jumper-Selectable Baud Rates:

| Rate | Deviation | Rate | Deviation |
|---|---|---|---|
| 50 | 0.0000% | 1800 | 0.0000% |
| 75 | 0.0000% | 2000 | 0.2532% |
| 110 | 0.0000% | 2400 | 0.0000% |
| 134.5 | 0.0166% | 3600 | 0.0000% |
| 150 | 0.0000% | 4800 | 0.0000% |
| 300 | 0.0000% | 7200 | 0.0000% |
| 600 | 0.0000% | 9600 | 0.0000% |
| 1200 | 0.0000% | 19200 | 3.1250% |

-External Baud Rate Input - DC to 880K baud

-Programmable Baud Rate - Jumper selected reference clock by timer counter. Range: 50 baud to 38400 baud, with maximum deviation of 1.7%.

## 2-5 Timer/Counters

Input Frequency 5.000 MHz ±0.01% (Requires 8254 or equivalent)
1.250 MHz ±0.01%
78.125 KHz ±0.01%

Event Rate - 2.46 MHz max.

## 2-6 Parallel Interface

An 8255 programmable peripheral interface (PPI) provides 24 bits of parallel I/O. These 24 lines are TTL compatible and can be programmed for either input or output. The 8255 supports three modes of operation: basic I/O; strobed I/O; and bi-directional bus.

## 2-7 iSBX Connectors

Two industry-standard iSBX connectors can accommodate two single-sized MULTIMODULE boards or one double-sized MULTIMODULE board.

## 2-8 MULTIBUS/IEEE 796 Compliance

Master D16 M24 I16 VOL

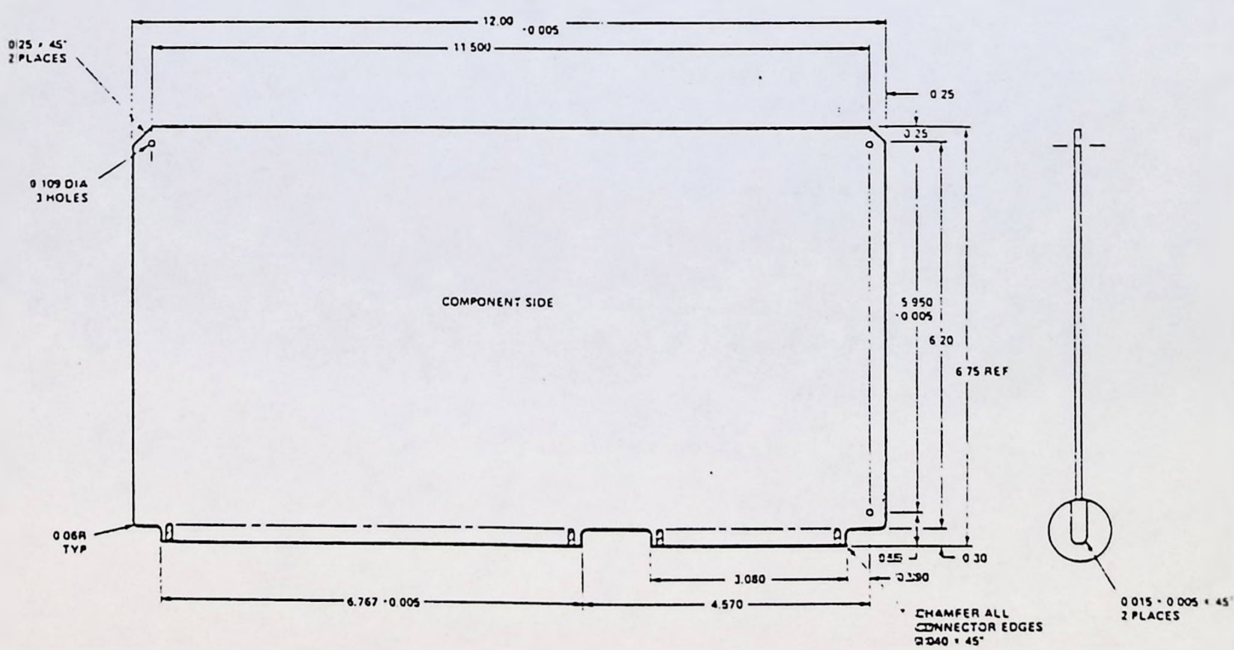
Slave D16 M24

BCLK/ and CCLK/ 10.0 MHz ±0.01%

## 2-9 Physical Characteristics

The printed circuit board is manufactured from natural color, NEMA grade FR-4 glass epoxy, approved to a minimum of UL-94V2. A solder mask is applied to component and solder sides, and component identification is silk screened on component side in white ink.

**Figure 2-9: M68K10 Dimensions**



## 2-10 Mating Connectors

Figure 2-10: I/O Header Mating Connectors

| Header | Use | Mating Connector |
|---|---|---|
| J1 | serial ports | 3M p.n. 3425-6050 or equivalent |
| J2 | parallel timer | 3M p.n. 3425-6050 or equivalent |
| J3 | Reset | Berg p.n. 65039-031 housing, plus 2 Mini-PV receptacles: p.n. 47712 |
| J20 | Mem. Expansion | Viking p.n. 0002920002 or equivalent |
| J31 | iSBX module connector | Viking p.n. 0002920002 or equivalent |
| J33 | iSBX module connector | Viking p.n. 0002920002 or equivalent |
| J40 | Battery Backup | Berg p.n. 65039-034 housing, plus 3 Mini-PV receptacles: p.n. 47712 |

## 2-11 Connector Pin Assignments

See section 5 for the pin assignments of the connectors on the M68K10.

## 2-12 Environmental Requirements

Operating Temperature - $0^{o}$ C to $70^{o}$ C
Relative Humidity - 0 to 95% (noncondensing)

## 2-13 Power Requirements

Typical currents at $\pm 5\%$ of specified voltage

| | +5V | +12V | -12V |
|---|---|---|---|
| Without EPROM<br>Without MXM10 | 2.7A | 17mA | 11mA |
| Without EPROM<br>With MXM10 | 2.9A | 17mA | 11mA |

## 2-14 Ordering Information

| Part Number | Description |
|---|---|
| M68K10 | MULTIBUS 68000 single-board computer with 128K bytes of RAM. |
| MXM10 | Add-on module to expand M68K10's on-board RAM by 128K bytes (to 256K bytes). Requires M68K10 for operation. |
| SDB-P | PROBUG high-performance software monitor/debugger. |
| MAN-68K10 | M68K10 reference manual (the one you are reading) for M68K10 boards with serial numbers 0 through 3328 and 3331 through 3727, inclusive. |
| MAN-PROBUG | PROBUG reference manual and command summary card. |
| CBL-68K10 | Serial cable for M68K10 board. |
| PTR-1E | Centronics parallel interface. |

# 3. PREPARATION FOR USE

This section describes the configuration options of the M68K10, and how to set up a MULTIBUS system for the M68K10.

## 3-1 Unpacking and Inspection

Before opening the shipping carton, inspect it carefully for damage. If it appears to be damaged or water-stained, you should request that the shipper's agent be present when the carton is opened. If the shipper's agent is not present when the carton is opened and the contents are damaged, retain the carton and packing materials for the agent's inspection. In fact, it is a good idea to retain the packing materials in any case, in the event that the board needs to be shipped.

If equipment must be returned for repair, contact SBE Customer Service for instructions and a Returned Material Authorization number.

## 3-2 Installation Considerations

### 3-2-1 Equipment Requirements

In order to use the M68K10 you may need additional equipment. Typically, this will include the following:

1. If the M68K10 is to be used with other MULTIBUS boards, a MULTIBUS backplane is required. If used alone, the M68K10 will require a connector compatible with the P1 edge connector, to allow power to be supplied to the board.

2. I/O connectors and cables.

3. A CPU bootstrap program must reside in on-board PROM. PROBUG, the high-performance debugger/monitor, supplies this bootstrap. (PROBUG must be ordered separately; specify part number SDB-P).

4. A power supply providing +5V, +12V, and -12V.

5. A terminal for communicating with the system.

### 3-2-2 Power Requirements

| | +5V | +12V | -12V |
|---|---|---|---|
| Standard M68K10 | 2.7A | 17mA | 11mA |
| Add for MXM10 128K Memory | 200mA | -- | -- |
| Add for 4 2716 devices | 100mA | -- | -- |
| Add for 4 2732 devices | 150mA | -- | -- |
| Add for 4 2764 devices | 180mA | -- | -- |

### 3-2-3 Cooling Requirements

Operating temperature range for the M68K10 is $0^\circ$ C to $70^\circ$ C. Forced air cooling may be required to maintain these operating conditions.

## 3-3 Standard Shipping Configuration

When you receive the M68K10, it will be jumpered for default RAM size, speed, and type, and many other settings. The default jumper settings are suitable for most applications; however, you can install or remove jumpers to suit your application.

The standard M68K10 board is jumpered as follows:

J21 Jumper area J21 is set for 8K by 8-bit memory components for the four 28-pin sockets. Write operations to sockets U5 and U35 are not enabled. (J21: A1 to B1.)

J4 Jumper area J4 is set for 400-500 ns EPROMs, and no wait states for on-board RAM access. (J4: A3 to B3; A6 to B6.)

J24, J22 Jumper areas J24 and J22 are set for 2764-type memory components in sockets U16 and U17. If you have ordered the PROBUG monitor-debugger, the 2764-type PROBUG PROMs are installed in those sockets. (J24 and J22: A1 to B1; B5 to B6; A7 to B7.)

J25, J23 Jumper areas J25 and J23, which correspond to sockets U5 and U35, are not jumpered for any particular memory type. (J25 and J23: no jumpers installed.)

J26 Jumper area J26 is jumpered for on-board power (no battery backup) for all four 28-pin RAM/EPROM sockets. (J26: A2 to A3; B2 to B3).

J17, J18 Jumper areas J17 and J18's settings assume that the MXM10 Memory Expansion Module, with 128K bytes of memory, is attached to the M68K10. (J17: A1 to B1. J18: A3 to B3; B1 to C1; B2 to C2.)

J28 Jumper area J28 is set so that the baud rates of both channel A and channel B are determined by the jumpering of J27, rather than by the counter/timer. (J28: A2 to A3; B2 to B3.)

J27 Jumper area J27 is set for 9600 baud for both channel A and channel B. (J27: A1 to B1; A1 to B1. That is, A1 to B1 on each half of jumper area.)

J34, J35 Jumper areas J34 and J35 are not jumpered; this assumes that no timer options are installed. (J34 and J35: no jumpers installed.)

J8 Jumper area J8 is set so that if timer/counters are connected, a 1.250 MHz clock frequency is assumed. (J8: A1 to B1.)

J7 Jumper area J7's setting assumes that the system clock source is on-board. (J7: 2 to 3.)

J15 Jumper area J15 is set so that the BCLK signal is supplied to the MULTIBUS. (J15: jumper installed.)

J16 Jumper area J16 is set so that the CCLK signal is supplied to the MULTIBUS. (J16: jumper installed.)

STANDARD SHIPPING CONFIGURATION

| | |
|---|---|
| J13 | Jumper area J13 is set so that the BPRO signal is supplied to the MULTIBUS, for serial priority. (J13: jumper installed.) |
| J36 | Jumper area J36 is set to accept the BPRN signal from the MULTIBUS. (J36: 2 to 3.) |
| J37 | Jumper area J37 is set so that the M68K10 will release the MULTIBUS only if requested to do so. (J37: 2 to 3.) |
| J14 | Jumper area J14 is set so that the INIT signal is supplied to the MULTIBUS. (J14: jumper installed.) |
| J10, J11 | Jumper areas J10 and J11 set the starting address of the M68K10's first 64K bytes of memory at location 0B0000 on the MULTIBUS. (J10: no jumpers installed. J11: A5 to B5; A7 to B7; A8 to B8.) |
| J6, J29 | Jumper areas J6 and J29 have no jumpers installed; thus no interrupts are enabled on the M68K10. (J6 and J29: no jumpers installed.) |
| J5 | Jumper area J5 is set to enable a bus error timeout on MULTIBUS accesses. (J5: jumper installed.) |

The remainder of section 3 describes how to change the M68K10's default jumper settings. If your application requires no jumper changes, you can skip section 3.

## 3-4 28-Pin Sockets For PROM/RAM

The M68K10's four 28-pin sockets U5, U35, U16 and U17 can be loaded with either 24- or 28-pin memory components. Sockets U16 and U17 must be loaded with PROM-based software containing initialization data for the 68000. The PROBUG debugger/monitor, which contains the appropriate initialization data, is often used in these sockets. The other two sockets, U5 and U35, may contain additional PROMs or RAMs of your choice.

Because the memory components that fit into 28-pin sockets are all 8 bits wide, they must be accessed in pairs to form a 16-bit word. The higher byte (bits 8 through 15) of the 16-bit word is assigned to sockets U5 and U16. The lower byte (bits 0 through 7) of the 16-bit word is assigned to sockets U17 and U35.

Some of the M68K10's default jumper settings apply to all four sockets, while others must be set individually for each pair of PROMs (or RAMs). For example, the jumpering for memory component size affects all four sockets whereas the jumpering for the memory component type controls each pair of PROM sockets individually.

Before loading any PROMs or RAMs in the sockets, you need to decide whether the standard jumperings are suitable for your applications. First, determine the speed and size, and whether you require battery backup for RAM. The jumpering for these characteristics will affect all four of the PROM/RAM sockets.

For sockets U5 and U35, we suggest that you select PROMs/RAMs that match the speed of the components in U16 and U17 fairly closely, since the jumpering for PROM access time affects all four of these sockets. If the speeds of the two pairs of memory components do not match, the board will have to be jumpered for the slower of the two types.

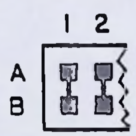
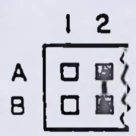
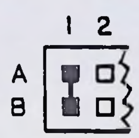
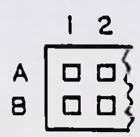
Note: With 28-pin EPROMs (8K or 16K), the M68K10 will not accommodate battery backed-up 8K x 8-bit RAMs.

### 3-4-1 Setting Memory Component Size

Rows 1 and 2 of jumper area J21 must be set to match the size of the largest component installed in U16, U17, U5 and U35. In the standard configuration, J21 is set for 8K x 8-bit components. Note that the size you select affects <u>all four</u> of the memory sockets.

If the components in U5 and U35 are a different size from those in U16 and U17, the larger components determine how you should jumper rows 1 and 2 of J21. For example, with 2K-byte PROMs and 8K-byte RAMs, use the jumpering shown in the "8K x 8" row of Figure 3-4-1. Note that this will leave a 12K-byte gap between the end address of the PROMs and the beginning address of the RAMs.

Figure 3-4-1: J21 Jumpering For Memory Component Size

| Component Size | Rows 1 and 2 Of Jumper Area J21 | Address Range U16 and U17 | Address Range U5 and U35 |
|---|---|---|---|
| 2K x 8 |  | FC0000 to FC0FFF | FC1000 to FC1FFF |
| 4K x 8 |  | FC0000 to FC1FFF | FC2000 to FC3FFF |
| 8K x 8 |  | FC0000 to FC3FFF | FC4000 to FC7FFF |
| 16K x 8 |  | FC0000 to FC7FFF | FC8000 to FCFFFF |

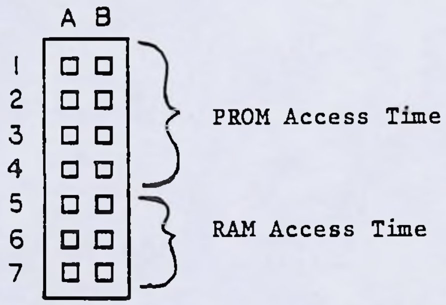
### 3-4-2 Setting PROM Access Time

To select the appropriate PROM access time for the 28-pin sockets, you may need to jumper rows 1-4 of the seven-row jumper area J4. In the standard configuration, J4 is set for 400-500ns PROMs. Note that the jumpering of J4 affects <u>all</u> <u>four</u> memory sockets.

(Rows 5-7 of jumper area J4 control the dynamic RAM access time; to set RAM access time, see section 3-5-2, **Setting Access Time For Dynamic RAM.**)

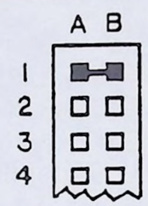
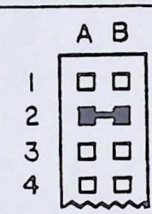
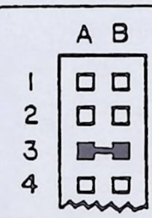
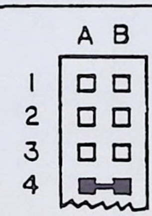
Figure 3-4-2a shows the pins of J4 and their corresponding functions.

Figure 3-4-2a: Jumper Area J4




When selecting the PROM access time, be sure to choose the speed for the slowest PROM on the board. Figure 3-4-2b (on the next page) shows how to jumper J4 for various PROM access times.

Figure 3-4-2b: J4 Jumpering For PROM Access Time

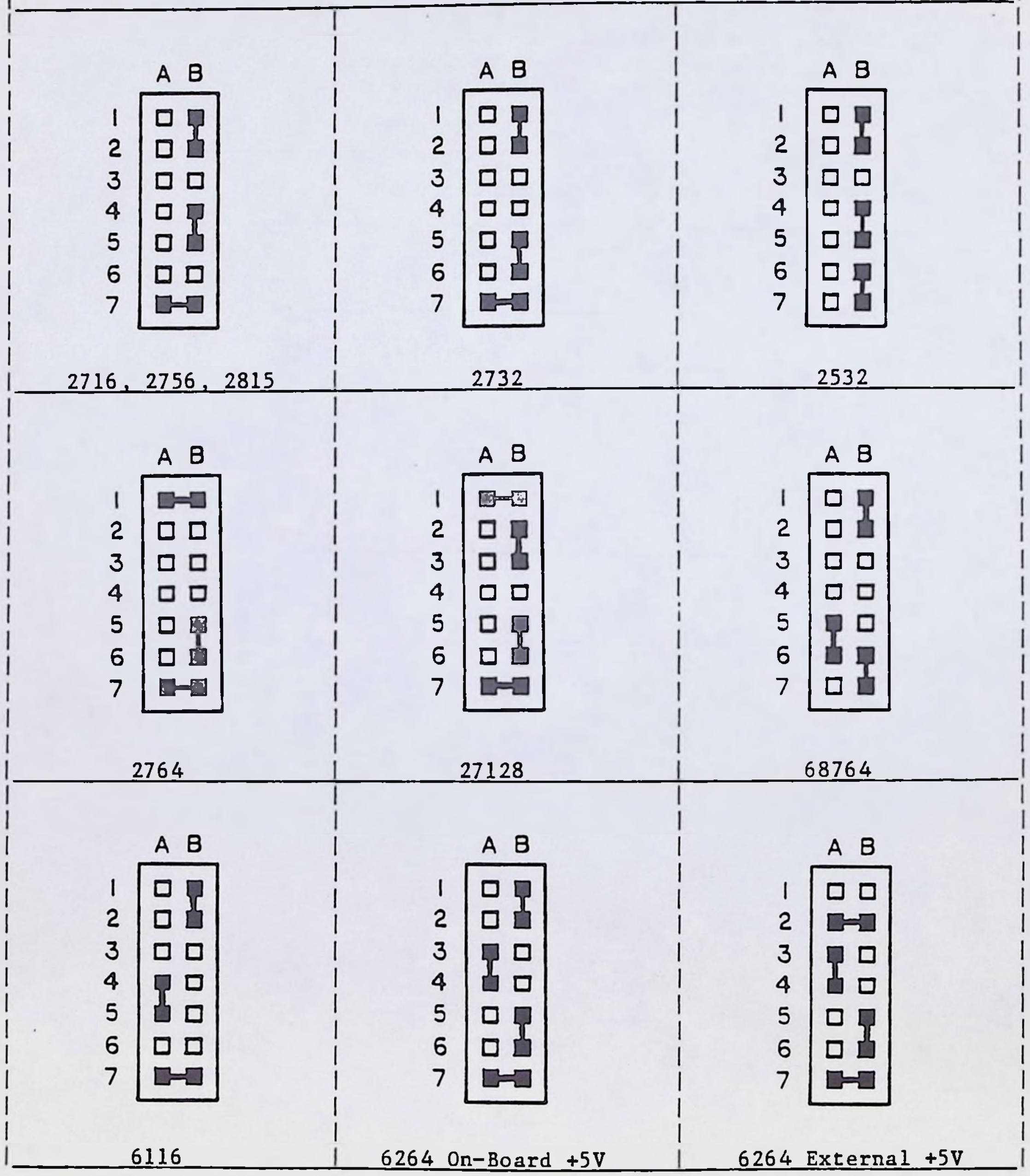
| PROM Access Time | Rows 1-4 Of Jumper Area J4 |
|---|---|
| < 300 nsec |  |
| 300-400 nsec |  |
| 400-500 nsec |  |
| 500-600 nsec |  |

### 3-4-3 Jumpering For Various PROM/RAM Types

Next to each of the 28-pin sockets (U5, U35, U16 and U17) is a 14-pin jumper area for configuring the socket for the PROM or RAM type to be installed. Jumper areas J25 and J23 correspond to sockets U5 and U35, respectively; jumper areas J24 and J22 correspond to sockets U16 and U17, respectively.

Each pair of sockets that you will load with memory components must have their corresponding jumper areas set up for the type of component to be installed. In the standard configuration, J24 and J22 are set for 2764-type PROMs. J25 and J23 are not set for any memory type.

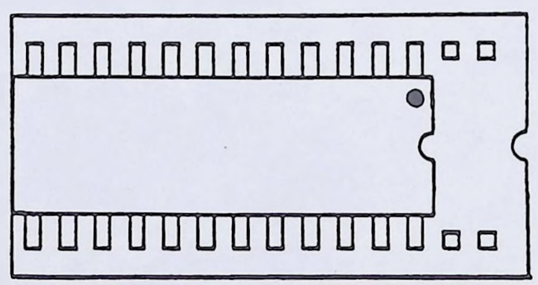
Figure 3-4-3: Jumpering Of J25, J24, J22 & J23
For Most Common PROMs And RAMs



### 3-4-4 How To Install 24-Pin Components In 28-Pin Sockets

To install 24-pin memory components in the 28-pin sockets, orient the M68K10 so that the MULTIBUS P1 and P2 connectors are at the bottom of the board. Install the 24-pin component so that its left edge is lined up with the left edge of the socket, placing pin 1 of the component in pin 3 of the socket. Do NOT attempt to match pin 1 of the component with pin 1 of the socket.

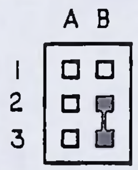
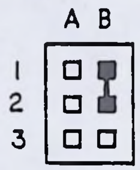
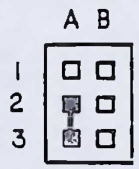
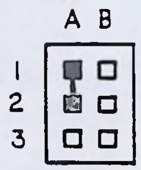
Figure 3-4-4: Position of 24-Pin Component In 28-Pin Socket



3-4-5 28-Pin Socket Battery Back-Up Option

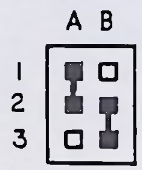
Each pair of 28-pin sockets may either be connected to on-board power, or powered from an external source through connector J40 (e.g., battery). Jumper area J26 selects between these two options. Figure 3-4-5a indicates the pins that should be connected for the various options. In the standard configuration, J26 is jumpered for on-board power for all four sockets.

Figure 3-4-5a: J26 Jumpering

| Socket Pair | On-Board Power | External Power |
|---|---|---|
| U16 & U17 |   |   |
| U5 & U35 |   |   |

For example, if you wanted sockets U16 and U17 to be driven by on-board power, and battery backup for sockets U5 and U35, you would jumper J26 as follows:

Figure 3-4-5b: Sample J26 Jumpering

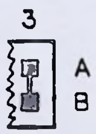


### 3-4-6 RAM Option For U5 and U35

Byte-wide static RAM components may be installed in U5 and U35. To enable write operations to these sockets, install a jumper between pins A3 and B3 of J21. The options described in sections 3-4-1 through 3-4-3 should be set up to match the RAM type and size.

In the standard configuration, write operations to sockets U5 and U35 are not enabled.

Figure 3-4-6: Row 3 Of J21
RAM Option For Sockets U5 & U35



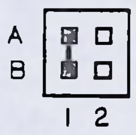
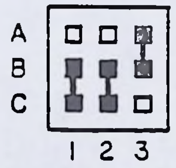
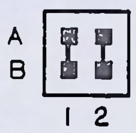
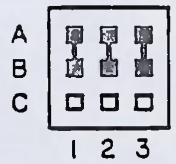
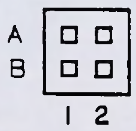
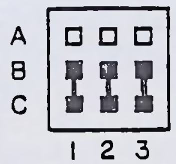
## 3-5 Jumpering For Dynamic RAMs

### 3-5-1 Installing MXM10 Dynamic RAM Expansion Module

To add 128K or 512K bytes of dynamic RAM to the M68K10, install the MXM10 memory expansion module on the M68K10 board. The MXM10 plugs into connector J20, which is to the right of socket U75. The MXM10 has a capacity of 128K bytes using 64K RAMs; with 256K RAMs, its capacity is 512K bytes.

With the MXM10 installed, J17 and J18 may need to be altered. Figure 3-5-1 shows the setup of J17 and J18. The standard configuration assumes that the MXM10 module is attached, with 128K bytes of memory.

Figure 3-5-1: MXM10 Installation Options

| Option | J17 Jumper Area | J18 Jumper Area |
|---|---|---|
| 128K MXM10 |  |  |
| 512K MXM10 |  |  |
| No MXM10 |  |  |

### 3-5-2 Setting Access Time For Dynamic RAM

**Jumper Area J4, Rows 5-7 - RAM Access Time Selection.** The jumpering of rows 5-7 of J4 controls the signal DTACK for RAM access by the 68000, and the MULTIBUS signal XACK for slave accesses. In the M68K10's standard shipping configuration, J4 is jumpered from A6 to B6; this setting is for RAMs with an access time of 150 nanoseconds (ns), and results in a 68000 memory cycle of 400 ns. The standard configuration is suitable for most applications.

When J4 is jumpered from A6 to B6 and a secondary master accesses on-board memory, the XACK signal is asserted when data appears on the MULTIBUS. If the MULTIBUS master is another M68K10 board, you can jumper J4 from A5 to B5 instead. This will cause XACK to be asserted before data appears on the MULTIBUS, saving 100 nanoseconds in the access. This does not meet MULTIBUS specifications, but will work if the secondary master is also an M68K10.

JUMPERING FOR DYNAMIC RAMS

If 200 ns RAMs are used, jumper J4 from A7 to B7.

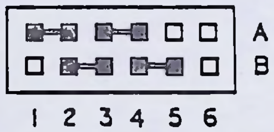
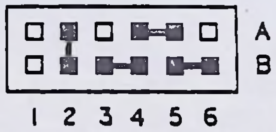
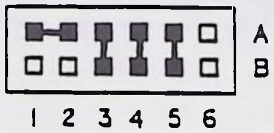
Figure 3-4-2a shows the pins of J4 and their corresponding functions. (Rows 1-4 of J4 control the PROM access time; see section 3-4-2.)

### 3-5-3 Jumpering For Clock Rates And RAM Speeds

The M68K10 is delivered with a 10 MHz clock and with 150 ns RAMs installed. For many purposes, the factory setup is appropriate. However, to use an 8 MHz clock rate or 200 ns RAMs, you will need to re-wire jumper area J19, which is hardwired for the 10 MHz clock and 150 ns RAMs. You should be familiar with the interfacing requirements of dynamic RAM before attempting to use a non-standard jumpering scheme.

Figure 3-5-3 shows the factory setup and two other useful options. J19 selects the timing of the dynamic RAM control signals RAS (RT), CAS (CT), and WE (WT), and when the addresses are multiplexed (MT).

Figure 3-5-3: Jumpering For Clock Rates And RAM Speeds

| | J19 Area | Delay From MAS |
|---|---|---|
| Factory Setup (hard wiring) | <br>10 MHz Clock, 150 ns RAMs | RT - 0<br>MT - 25ns<br>CT - 50ns<br>WT - 75ns |
| Option 1 | <br>10 MHz Clock, 200 ns RAMs | RT - 25ns<br>MT - 75ns<br>CT - 100ns<br>WT - 125ns |
| Option 2 | <br>8 MHz Clock, 150-200 ns RAMs | RT - 0<br>MT - 50ns<br>CT - 75ns<br>WT - 100ns |

## 3-6 Serial I/O Options

The baud rates for serial I/O channels A and B are independently selectable. For each channel, there are two sources that can determine the baud rate: the jumpering of J27 and the output of timer 2.

Jumper area J28 selects between these two sources for each channel. Jumper area J27 selects among 16 standard baud rates between 50 baud and 19.2K baud.

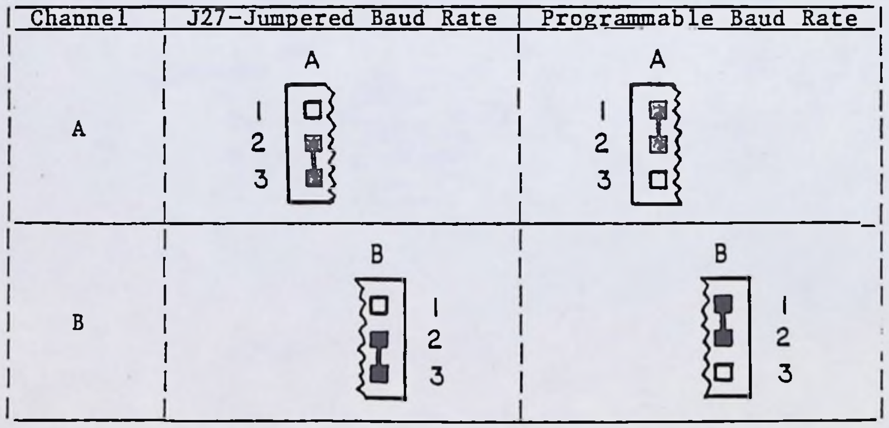
### 3-6-1 Selecting Between Jumpered And Programmable Baud Rate

The baud rates of channels A and B can be selected either by jumper area J27, or by the counter/timer. The jumpering of J27 is covered in section 3-6-2. See the programming examples in section 4 for information on setting up the counter/timer for programmable baud rates.

In the standard configuration, J28 is jumpered so that both channels' baud rate is selected by J27, rather than by the counter/timer. To select between the baud rate determined by the jumpering of J27 and a programmable baud rate, set jumper area J28 as follows:

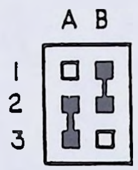
Figure 3-6-1a: Jumper Area J28

PORT A - PRINT
PORT B - KYBD




For example, to set channel A with the baud rate determined by J27, but set channel B's baud rate under program control, you should set jumper area J28 as follows:

Figure 3-6-1b:
Sample J28 Jumpering




### 3-6-2 Serial I/O Baud Rate Selection

Jumper area J27 is used to set jumper-selectable baud rates. The "top half" of J27 controls channel A; the "bottom half" controls channel B. In the standard configuration, J27 is jumpered for 9600 baud on both channels.

The following sample of J27 jumpering would set channel A to run at 1200 baud and channel B to run at 9600:

Figure 3-6-2a: Sample J27 Jumpering

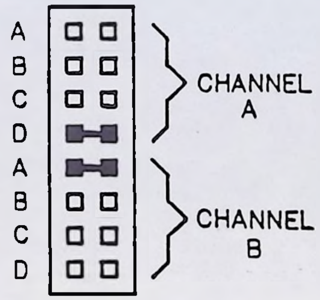
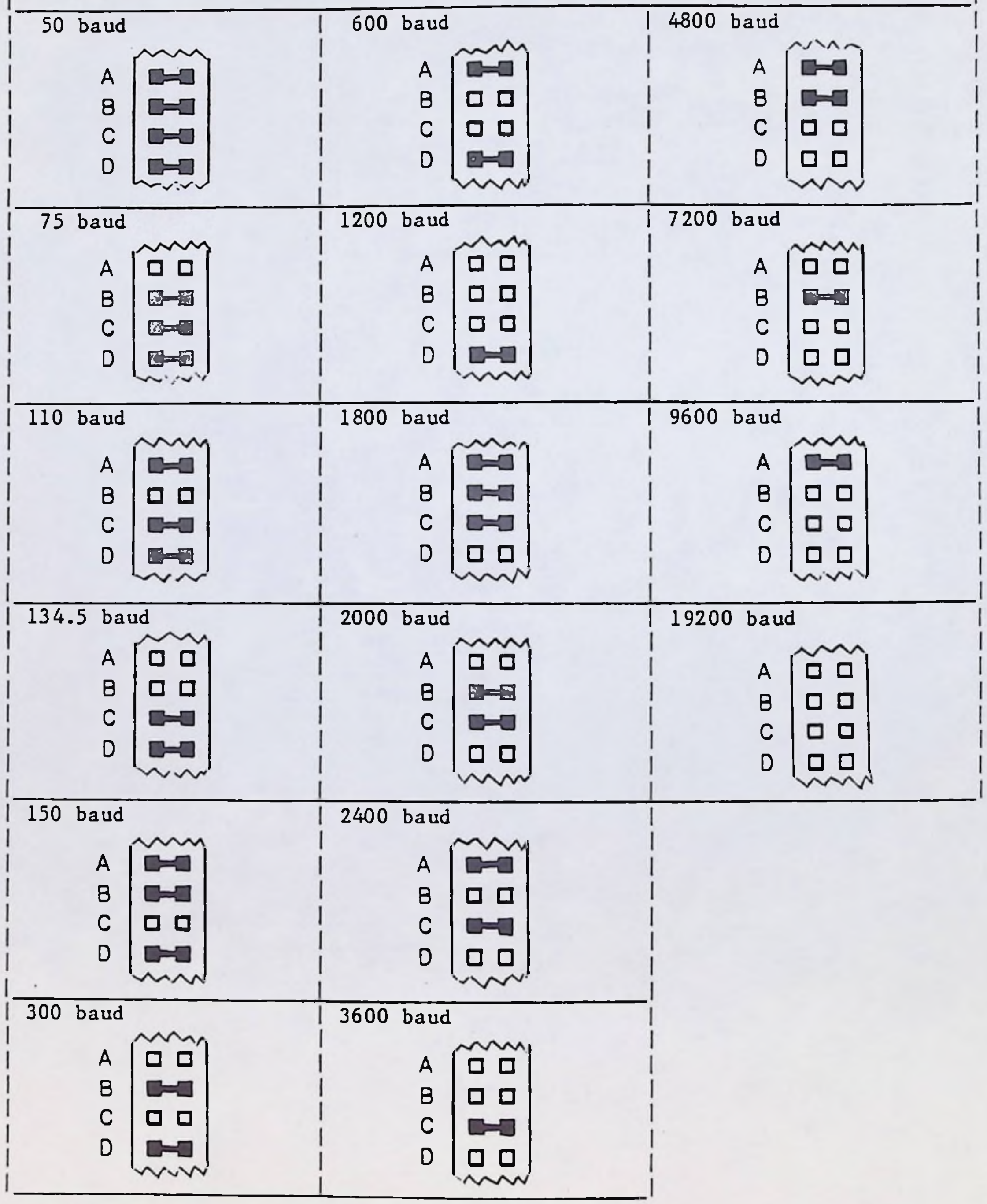



Figure 3-6-2b, on the next page, shows the jumper settings for each of the sixteen possible baud rates. Note that the output frequency of the baud rate generator is sixteen times the actual baud rate; the 8274 is initialized to operate with a times sixteen input.

Figure 3-6-2b: Jumper Settings For Each Baud Rate (Halves of J27)



## 3-7 Parallel and Timer I/O Options

Jumper areas J34 and J35 are used to select the clock and gate input sources for counter/timer sections 0 and 1, and to select the function of J2 header pins 30 and 32. In the standard configuration, no jumpers are installed in J34 and J35; this assumes that no timers are connected to the M68K10.

Figure 3-7-1 identifies the pins of J34 and J35. Figure 3-7-2 shows the signals on each pin, and figures 3-7-3 and 3-7-4 describe some useful options.

Figure 3-7-1: Pin Locations On Jumper Areas J34 & J35

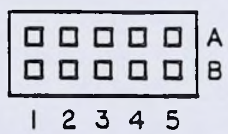



Figure 3-7-2: Signals On J34 & J35

| J34 Pin | Signal |
|---|---|
| A1 | Fixed clock rate from J8 |
| A2 | Output of timer 1 |
| A3 & A4 | Pin 32 of J2 |
| A5 | Gate of timer 1 |
| B1, B2 & B3 | Clock input of timer 0 |
| B4 | PC7 of 8255 |
| B5 | Gate of timer 1 |
| **J35 Pin** | **Signal** |
| A1 | Fixed clock rate from J8 |
| A2 | Output of timer 0 |
| A3 & A4 | Pin 30 of J2 |
| A5 | Gate of timer 0 |
| B1, B2 & B3 | Clock input of timer 1 |
| B4 | PC6 of 8255 |
| B5 | Gate of timer 0 |

Figure 3-7-3: Timer Clock & Gate Options

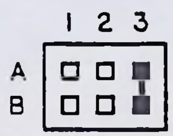
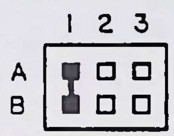
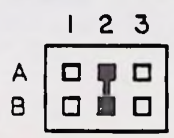
| Clock Input Option | Jumpers |
|---|---|
| Fixed clock rate from J8 | A1 to B1 |
| Output from other timer | A2 to B2 |
| External clock from J2 | A3 to B3 |
| Output from 8255 | B3 to B4 |
| **Gate Input Option** | **Jumpers** |
| Gate always enabled | None |
| Output from 8255 | B4 to B5 |
| External gate from J2 | A4 to A5 |

Figure 3-7-4: J2 Header I/O Options

| J2 Pin Function | Jumpers |
|---|---|
| Timer output | A2 to A3 |
| Timer clock input | A3 to B3 |
| Timer gate input | A4 to A5 |
| 8255 I/O | A4 to B4 |

The on-board source for the timer clock inputs is selected by jumpers at J8. Figure 3-7-5 shows the jumpering of J8 for each of the three options. In the standard configuration, J8 is jumpered for a 1.250 MHz clock frequency.

Figure 3-7-5
On-Board Timer Clock Source Options

| Clock Frequency | Jumper Area J8 |
|---|---|
| 5.000 MHz (requires 8254 or equivalent for operation) |  |
| 1.250 MHz |  |
| 78.125 KHz |  |

## 3-8 MULTIBUS Options

**Single-Master System.** A single-master MULTIBUS system is one in which only one master is installed on the MULTIBUS. A master can be either a microprocessor card such as the M68K10, or an I/O card that can take control of the bus in order to transfer data directly to memory. In a single-master system, only the master can control the bus.

**Multi-Master System.** A multi-master system contains more than one card that can function as master of the MULTIBUS: for example, a system with two M68K10s, or an M68K10 and a disk controller with master capabilities.

Because the M68K10's dynamic RAM is dual-ported, the M68K10 is well-suited to multi-master systems, in which I/O controllers with master capabilities can do DMA transfers to and from the M68K10's memory. Dual-ported RAM is also useful in environments where the processors need to communicate with each other.

In a multi-master system, only one master (an M68K10) drives the signals INIT, BCLK, and CCLK. This master is referred to as the **primary master**. The other masters in the system, the **secondary masters**, must be set up to receive the INIT, BCLK, and CCLK signals from the primary master.

In a multi-master system, a serial or a parallel priority scheme is used to determine which master will have access to the MULTIBUS. If the system has only two or three masters, the serial priority scheme may be used, and the BPRN signal on the highest priority master must be connected to ground. If the system has more than three masters, the parallel scheme must be used.

In a serial priority scheme, the priority of each master is determined by slot position in the MULTIBUS card cage: the highest-priority master resides in the first slot, the second-priority master resides in the second slot, etc. In a parallel priority scheme, the priority of each master is determined by a parallel priority encoder on the MULTIBUS backplane.

Note that the highest-priority master in a multi-master system is not necessarily the primary master. In other words, the board receiving highest priority for MULTIBUS accesses does not necessarily drive the INIT, BCLK and CCLK signals.

**Standard Configuration.** In the standard configuration, the M68K10 is jumpered as follows:

J7 assumes that the system clock source is on-board. J15 and J16 are set so that the BCLK and CCLK signals are supplied to the MULTIBUS.

J13 is set to supply the BPRO signal to the MULTIBUS (for serial priority). J36 is set to accept the BPRN signal from the MULTIBUS, and J37 is set so that the M68K10 will release the MULTIBUS only if requested to do so.

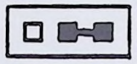
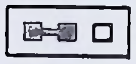
Jumper area J14 is set so that the INIT signal is supplied to the MULTIBUS.

Figure 3-8: MULTIBUS Option Jumper Areas & Corresponding Functions

| Jumper Area | Function |
|---|---|
| J7 | Selects between on-board and external clock source |
| J10 | Selects on-board slave memory address |
| J11 | Selects MULTIBUS slave memory address |
| J13 | Connects BPRO to MULTIBUS |
| J14 | Connects INIT to MULTIBUS |
| J15 | Connects BCLK to MULTIBUS |
| J16 | Connects CCLK to MULTIBUS |
| J36 | Connects BPRN input to MULTIBUS or Ground |
| J37 | Connects CBRQ input to MULTIBUS or Ground |

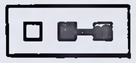
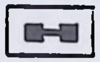
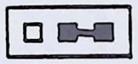
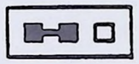
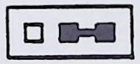
## 3-8-1 Clock Option Jumpering

Figure 3-8-1: Clock Option Jumpering

| | J7 | J15 | J16 |
|---|---|---|---|
| Single MULTIBUS Master, OR Primary Master In Multi-Master System |  1 2 3 Clock Source On-Board |  BCLK Connected |  CCLK Connected |
| NON-Primary Master In Multi-Master System |  1 2 3 External Clock Source |  BCLK Not Connected |  CCLK Not Connected |

### 3-8-2 Bus Priority Jumpering

Figure 3-8-2: Bus Priority Jumpering

| | MULTIBUS BPRO Signal | MULTIBUS BPRN Signal | MULTIBUS CBRQ Signal |
|---|---|---|---|
| Single-Master System | J13 jumpering doesn´t matter |  1 2 3<br>Jumper Area J36: MULTIBUS Priority (BPRN) Always Granted |  1 2 3<br>Jumper Area J37: MULTIBUS CBRQ Input Always Active |
| Multimaster System: Serial Priority Scheme | <br>Jumper Area J13: BPRO Connected |  1 2 3<br>Jumper Area J36: BPRN Conn. For Not Highest Prior. Master<br> 1 2 3<br>Jumper Area J36: * BPRN To Ground For Highest Prior. Master | Depends On Use ** |
| Multimaster System: Parallel Priority Scheme | <br>Jumper Area J13: BPRO Not Connected |  1 2 3<br>Jumper Area J36: BPRN Always Connected | Depends On Use ** |

* This is necessary only if the BPRN signal is not grounded on the backplane.

** See section 3-8-4 for a discussion of how to jumper J37 for your application.

### 3-8-3 Reset Options

There are three ways to reset the M68K10:

(1) Power-up the M68K10 (full Reset)
(2) Press the Reset button, connected to pins 1 and 2 of connector J3 (full Reset) (see figure 5-4)
and (3) Use a 68000 Reset instruction (partial Reset).

A "full Reset" means that the I/O devices, the two iSBX connectors, and the 68000 processor all receive a Reset pulse. A "partial Reset" occurs when the 68000 executes a Reset instruction. A partial Reset causes the I/O devices and the two iSBX connectors receive a Reset pulse. The 68000 processor does not receive a Reset pulse during a partial Reset.

Jumper area J14 allows the M68K10 to drive the INIT signal during a full Reset. If you install a jumper in this two-pin area, the Reset switch will initialize the MULTIBUS. If J14 is not jumpered, the M68K10 will not drive the INIT signal.

### 3-8-4 Relinquishing MULTIBUS Mastership

Jumper area J37 selects the action taken by the M68K10 following each MULTIBUS access. The MULTIBUS signal CBRQ allows the current master to sense whether any other master needs the bus, and likewise allows lower priority masters to signal that the current master must relinquish the bus (if the current master is not using the bus).

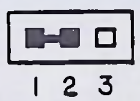
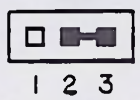
J37 may be jumpered so that the M68K10 senses CBRQ as always active, and thus gives up mastership of the bus following each MULTIBUS access. This allows other masters more use of the MULTIBUS, but results in slower bus access for the M68K10 (since bus arbitration is required for each M68K10 access).

If J37 is jumpered so the M68K10 senses CBRQ as driven by the other masters, bus arbitration is only required if another master needs to use the bus; otherwise, the M68K10 remains bus master between accesses, and bus arbitration is not required for each access. This latter option is recommended, and is the standard configuration.

In the standard configuration, a high-priority master will not release the bus to lower-priority masters until an on-board access occurs. This can cause bus "hogging" on the part of the high-priority master, unless high-priority masters access the bus only for short periods of time (e.g., for short bursts of DMA). Likewise, if a master will be executing code on the MULTIBUS, it should be assigned a low priority.

For example, as the highest-priority master, the M68K10 can fully saturate the MULTIBUS while executing a program on the MULTIBUS. This prevents lower-priority masters from gaining access to the bus as long as the program is running.

Figure 3-8-4: J37 Jumpering
Release Of MULTIBUS

| Option | Jumper Area J37 |
| --- | --- |
| M68K10 releases MULTIBUS after each access |  |
| M68K10 releases MULTIBUS only if requested to do so |  |

### 3-8-5 Slave Memory Option Selection

When the M68K10 operates in a multi-master system, other masters may access on-board dynamic RAM in blocks that are 64K bytes or larger. Note that neither on-board I/O nor the 28-pin sockets are accessible from the MULTIBUS.

## MULTIBUS OPTIONS

Jumper areas J10 and J11 select the addressing of the block of dual-ported memory to be accessed. In the standard configuration, the starting address of the M68K10's first 64K bytes of memory is at location $0B0000 on the MULTIBUS, selecting a 64K-byte block of MULTIBUS memory.

Jumper area J11 selects the location of the block of dual-ported memory within the MULTIBUS address space. If the M68K10 tries to access this block of MULTIBUS memory, a bus error exception will occur since the M68K10 cannot use the MULTIBUS to access its own on-board memory.

By default, jumper area J11 selects a 64K-byte block of MULTIBUS memory. With 24-bit addressing, there are 256 possible 64K-byte blocks, selected by the upper 8 address lines.

To jumper area J11, determine the upper 8 bits of the 64K-byte block's starting address. For example, if the starting address were $3A0000, its binary representation would be:

```
 0  0  1  1  1  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
|-------upper 8 bits-----|
```

For each of the address bits, there is a corresponding address line: the uppermost bit corresponds to A23, the next bit to A22, etc. Thus the upper 8 bits (in this example, 00111010) correspond to address bits A23-A16.

Each "0" indicates that there should be NO jumper connection for the corresponding address bit; each "1" indicates that there should be a jumper connection.

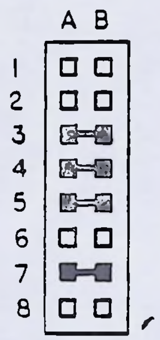
Use Figure 3-8-5a to determine the appropriate jumpering:

Figure 3-8-5a:
Dual-Ported RAM MULTIBUS Address Selection

| Address Bit | MULTIBUS Signal Name | J11 Jumper |
|---|---|---|
| A16 | ADR10 | A8 to B8 |
| A17 | ADR11 | A7 to B7 |
| A18 | ADR12 | A6 to B6 |
| A19 | ADR13 | A5 to B5 |
| A20 | ADR14 | A4 to B4 |
| A21 | ADR15 | A3 to B3 |
| A22 | ADR16 | A2 to B2 |
| A23 | ADR17 | A1 to B1 |

Continuing with the example (a starting address of $3A0000), jumper area J11 would look like this:

Figure 3-8-5b: Sample J11 Jumpering




Jumper area J10 selects which 64K-byte block of on-board dual-ported memory will reside on the MULTIBUS. The maximum amount of on-board dynamic RAM is 1 Megabyte, resulting in 16 possible 64K-byte blocks. Not all M68K10s will have 1 Megabyte of RAM installed; if less RAM is installed, only those blocks which actually exist as on-board dynamic RAM may be accessed from the MULTIBUS.

To set up J10 for the selected 64K-byte block, determine the second 4 bits of the 64K-byte block's on-board starting address. For example, using the starting address $010000, the binary representation of the upper 8 bits is 00000001; so the second 4 bits are 0001.

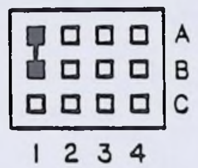
Using Figure 3-8-5c, install a jumper in J10 for each bit that is a '1'; do not install a jumper for any bit that is a '0'.

Figure 3-8-5c: Dual-Ported On-Board Address Selection

| Address Bit | J10 Jumper |
|---|---|
| A16 | A1 to B1 |
| A17 | A2 to B2 |
| A18 | A3 to B3 |
| A19 | A4 to B4 |

In the above example, jumpers should be installed in J10 from A1 to B1:

Figure 3-8-5d: Sample J10 Jumpering




## Selecting Memory Blocks Larger Than 64K Bytes

To select a block size larger than 64K bytes, you need to connect two pins on jumper area J10 to a pin on jumper area J11.

MULTIBUS address lines A16 to A19 (ADR10 to ADR13) correspond to pins C1-C4 (respectively) of jumper area J10. These signals may be connected to pins along the "B" row of jumper areas J10 and J11 to select the block size for more than 64K bytes of dual-ported memory.

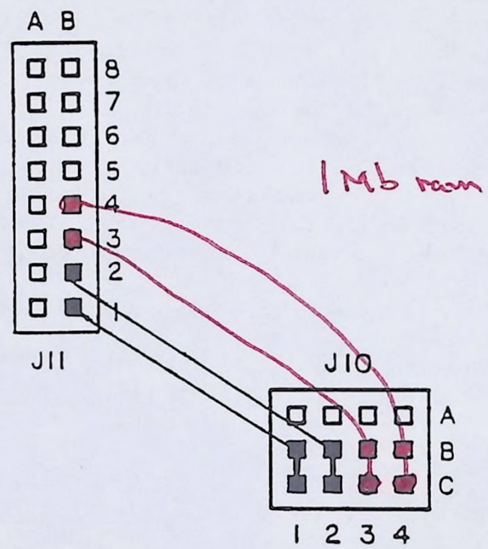
Figure 3-8-5e shows the block sizes.

Figure 3-8-5e:
Optional Block Sizes For Dual-Ported RAM

| Block Size | Jumpers |
|---|---|
| 128K | J10/C1 to J10/B1 and J11/B1 |
| 256K | J10/C1 to J10/B1 and J11/B1<br>J10/C2 to J10/B2 and J11/B2 |
| 512K | J10/C1 to J10/B1 and J11/B1<br>J10/C2 to J10/B2 and J11/B2<br>J10/C3 to J10/B3 and J11/B3 |
| 1M | J10/C1 to J10/B1 and J11/B1<br>J10/C2 to J10/B2 and J11/B2<br>J10/C3 to J10/B3 and J11/B3<br>J10/C4 to J10/B4 and J11/B4 |

For example, for 256K bytes of memory, jumper areas J10 and J11 as follows:

Figure 3-8-5f: Sample J10 & J11 Jumpering For More Than 64K Bytes




## 3-9 Disabling On-Board RAM

On-board RAM may be disabled, forcing all 68000 accesses in the range $000000 to $FBFFFF to be directed to the MULTIBUS. To disable on-board RAM, connect the B1 pin of jumper area J18 to a high logic level. (See Figure 3-5-1 for J17 and J18 jumper schemes.) Any "B" side pin of J11 may be used as a source of the high logic level, as long as it is not pulled to ground by jumpering to the "A" side. See section 3-8-5 for more information on jumper area J11.

## 3-10 Interrupt Options

The M68K10 has ten on-board sources of interrupts. In addition, MULTIBUS interrupt lines INT0 to INT5 may be used as interrupt sources. The 68000 provides seven levels (levels 1-7) of prioritized interrupts. Level 7, the highest priority, is non-maskable and is dedicated to pushbutton switch S1, located in the upper right-hand corner of the M68K10.

The M68K10 uses the autovector method of providing the 68000 with the interrupt service routine's address. With this method, the address of the service routine is stored in exception vector numbers 25 to 31, and the device requesting the interrupt does not have to provide a vector number to the 68000. The priority level is used to determine the vector number: vector #25 corresponds to priority level 1, vector #26 to priority level 2, etc.

**How To Assign Priority Levels For Interrupts.** To assign priority levels 1-6, you should first determine which processes are the most time-critical. These should be assigned the higher-priority interrupts, while the least time-critical processes should be assigned the lower-priority interrupts.

Priority level 7, which uses vector #31, is hardwired to switch S1.

Priority levels 1-6 can be connected either to the MULTIBUS signals INT5 to INT0, or to one of the on-board interrupt sources. Jumper area J6 controls these connections.

Jumper area J6 contains three rows (A, B, and C) and six columns (1-6). The columns represent priority levels 1-6, respectively (priority level 7 is hardwired to the S1 switch and cannot be set with J6).

Row A of jumper area J6 connects to on-board interrupts; row C connects to MULTIBUS interrupts. For example, if you connect jumper A2 to jumper B2, interrupt level 2 will be on-board; if you connect jumper C2 to jumper B2, interrupt level 2 will be generated from MULTIBUS line INT4.

The on-board interrupt sources are selected at jumper area J29. The nine pins on the "A" side of J29 are the sources of on-board interrupts. Except for the interrupt request from the serial I/O controller (8274) on pin A3, all of these sources are high when requesting an interrupt.

Six of the "B" side pins of J29 connect to the inputs of an open-collector inverter (74LS05) which converts the high-active interrupt requests to low active signals on the pins of J6.

You can connect more than one interrupt source to any destination on J6; this allows several interrupts to share the same priority level.

Note that A3 of J29 does not require an inverter since its serial I/O interrupt is low active. To use the 8274 serial I/O controller as an interrupt source, you need to install a wire from A3 of J29 to the appropriate "B" pin of J6.

## 3-10-1 Sources Of On-Board Interrupts

**Figure 3-10-1a: Sources Of On-Board Interrupts, & Corresponding J29 Pins**

| Interrupt source | J29 Pin |
|---|---|
| J33 iSBX MINTR0 | A1 |
| J33 iSBX MINTR1 | A2 |
| Serial I/O controller interrupt (low active) | A3 |
| Counter/Timer OUT1 | A4 |
| J31 iSBX MINTR0 | A5 |
| Counter/Timer OUT0 | A6 |
| J31 iSBX MINTR1 | A7 |
| 8255 PC3 | A8 |
| External source on J2 pin 50 | A9 |

Figure 3-10-1b shows the relationships between J29, U67 (the inverter), J6, and the interrupts.

**Figure 3-10-1b: Conceptual Illustration Of Interrupt System**

ON-BOARD INTERRUPTS — OFF-BOARD INTERRUPTS

| On-Board Interrupt Source | J29 Pins | | U67 Inverter | Pins Of Jumper Area J6 (LOWEST priority) | | | MULTIBUS Interrupts |
|---|---|---|---|---|---|---|---|
| Counter/Timer OUT1 | A4 | B4 | ---▷o--- | --- A1 | B1 | C1 --- | --- INT5 |
| Counter/Timer OUT0 | A6 | B6 | ---▷o--- | --- A2 | B2 | C2 --- | --- INT4 |
| J31 iSBX MINTR0 | A5 | B5 | ---▷o--- | --- A3 | B3 | C3 --- | --- INT3 |
| J31 iSBX MINTR1 | A7 | B7 | ---▷o--- | --- A4 | B4 | C4 --- | --- INT2 |
| 8255 PC3 | A8 | B8 | ---▷o--- | --- A5 | B5 | C5 --- | --- INT1 |
| Serial I/O Controller Int. | A3 | B3 | ---▷o--- | --- A6 | B6 | C6 --- | --- INT0 |
| J33 iSBX MINTR0 | A1 | B1 | --- N.C. | | HIGHEST Priority | | |
| J33 iSBX MINTR1 | A2 | B2 | --- N.C. | | | | |
| External source On J2 Pin 50 | A9 | B9 | --- N.C. | | | | |

Note: In Figure 3-10-1b, J29's pins are not shown in their actual (physical) order. The pins of jumper area J6, however, do appear in order.

How To Jumper Areas J6 and J29. After deciding what devices will require interrupts and determining the relative interrupt priority of each device, use Figure 3-10-1b to determine how to jumper area J6 (and area J29, for on-board interrupt levels) to suit your application. In the standard configuration, no interrupts are enabled on the M68K10.

To set up an on-board interrupt, connect the interrupt source on the A side of J29 to the inverter input for the desired priority level on the B side, and jumper J6 from A to B for the same level. (Exception: to use the 8274 serial I/O controller as an interrupt source, install a wire from A3 of J29 to the desired "B" pin of J6.)

For example, suppose you want timer #1 to interrupt the processor at priority level 1. You would start by installing a jumper between pins A4 and B4 of jumper area J29. This sends the interrupt signal to the inverter and the inverted signal to pin A1 of jumper area J6. Then, you would install a jumper between pins A1 and B1 of jumper area J6. This sets interrupt level 1 to be on-board.

If you wanted timer #1 to interrupt the processor at priority level 2, you could still start by jumpering A4 and B4 of J29. On J6, you would need to connect pin A1 to pin B2 to set priority level 2. Since a jumper plug can only connect contiguous pins, this would require wire-wrapping.

To receive a MULTIBUS interrupt, connect the MULTIBUS INT signal on the C row of J6 to desired level on the B row: B1 for level 1, B2 for level 2, etc.

### 3-10-2 How To Generate Interrupts On The MULTIBUS

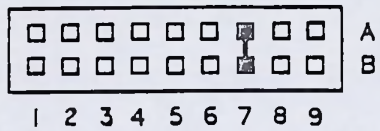
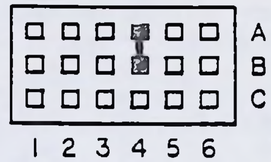
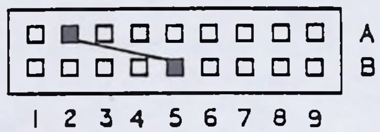
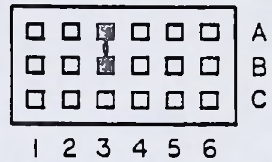
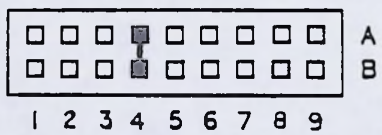
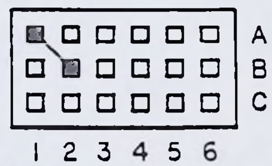
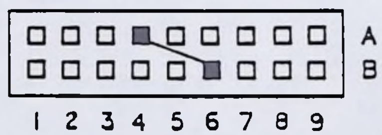
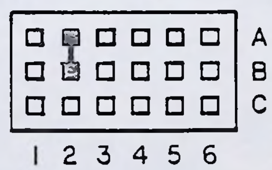
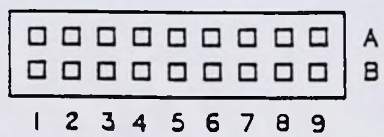
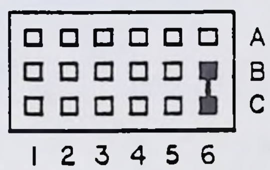
The M68K10 board can generate interrupts on the MULTIBUS under program control. The PC3 line of the 8255 (the Programmable Peripheral Interface) can be jumpered to control a MULTIBUS interrupt line.

For example, to allow the M68K10 to generate INT1 by writing a "1" to the PC3 line, install a jumper between pins A8 and B8 of J29, and connect pins A5 and C5 of J6. When the "1" is written into PC3, it goes to J29 pin A8, which is jumpered to pin B8. The signal then travels through an inverter, coming out on J6 pin A5, which is jumpered to pin C5. C5 drives the INT1 line on the MULTIBUS. INT1 is low active.

See the programming examples in section 4 for more information.

The following figure shows some more examples of J6 and J29 jumpering.

Figure 3-10-2: Examples Of J29 And J6 Jumpering

| Task | Jumper Area J29 | Jumper Area J6 |
|---|---|---|
| Set J31 iSBX MINTR1 at interrupt priority level 4 |  |  |
| Set J33 iSBX MINTR1 at interrupt priority level 3 |  |  |
| Set Counter/Timer OUT1 at interrupt priority level 2 (OPTION 1) |  |  |
| Set Counter/Timer OUT1 at interrupt priority level 2 (OPTION 2) |  |  |
| Set MULTIBUS interrupt INTO at priority level 6 |  |  |

If you have a choice as to how to jumper J6 and J29, you should choose the easiest pathway to the desired priority level. For example, avoid wire-wrapping two wires to the same pin if there is another way to wire one of the pins. If possible, use jumper plugs instead of wire-wrapping.

If it makes no difference whether you select one priority level or the one just above or below it, and if one requires wire-wrapping while the other requires only the use of jumper plugs, we recommend using the level that requires only jumper plugs.

## 3-11 Bus Error Time-out

Jumper area J5 may be jumpered to cause a bus error exception if a 68000 data access is not acknowledged within approximately 3 seconds. Since failure to acknowledge a data access is usually a fatal error, this feature allows the system to save information about the cause of the error. If J5 is not jumpered, the 68000 will wait forever for the acknowledgment; this is occasionally useful when debugging hardware problems.

In the standard configuration, J5 is set to enable a bus error timeout on MULTIBUS accesses.

# 4. PROGRAMMING INFORMATION

## 4-1 Memory Addressing

The M68K10 supports 24-bit addressing, resulting in an addressing range of 16 Megabytes. The upper four address lines are assigned to the P2 connector, which is the right hand group of gold-plated "fingers" on the bottom edge of the board.

To use 24-bit addressing on the MULTIBUS, you need to bus the four P2 address lines along the length of the backplane. If the M68K10 is installed in a backplane that does not bus the signals of the P2 connector, MULTIBUS memory addressing is limited to the lowest 1 Megabyte.

The M68K10 can contain up to 1 Megabyte of on-board dynamic RAM. Provided that you have not disabled this memory, it always starts at address $000000 and is a contiguous block. MULTIBUS memory begins where on-board dynamic RAM ends, and extends up to address $FBFFFF. The upper 256K bytes of memory, which begins at address $FC0000, is used for on-board I/O, the four 28-pin sockets and the 64K bytes of MULTIBUS I/O space. Figure 4-1a shows the organization of memory.

| Figure 4-1a: M68K10 Memory Map |
|---|
| $FF0000 to $FFFFFF Unused |
| $FE0000 to $FEFFFF MULTIBUS I/O |
| $FD0000 to $FDFFFF On-board I/O |
| $FC0000 to $FCFFFF 28-pin sockets |
| Top of on-board RAM to $FBFFFF<br>MULTIBUS Memory |
| On-board RAM |

Figure 4-1b: On-Board RAM Address Range

| Memory Option | Address Range |
|---|---|
| 512K M68K10 + 512K MXM10 | $000000 to $0FFFFF |
| 512K M68K10 only | $000000 to $07FFFF |
| 128K M68K10 + 128K MXM10 | $000000 to $03FFFF |
| 128K M68K10 only | $000000 to $01FFFF |

## 4-2 On-Board Input/Output Addressing

On-board I/O occupies a 64K block of memory beginning at address $FD0000. Figure 4-2 shows detailed information about on-board I/O addresses.

Figure 4-2: On-Board I/O Addressing

| Device | Address | Read | Write |
|---|---|---|---|
| 8274 | $FD0000 | Ch. A Data | Ch. A Data |
| MPSC | $FD0002 | Ch. B Data | Ch. B Data |
| | $FD0004 | Ch. A Status | Ch. A Command |
| | $FD0006 | Ch. B Status | Ch. B Command |
| 8255 | $FD0100 | Read Port A | Load Port A |
| PPI | $FD0102 | Read Port B | Load Port B |
| | $FD0104 | Read Port C | Load Port C |
| | $FD0106 | Invalid | Load Control Register |
| 8253 | $FD0200 | Read Counter A | Load Counter A |
| Timer | $FD0202 | Read Counter B | Load Counter B |
| | $FD0204 | Read Counter 2 | Load Counter 2 |
| | $FD0206 | Invalid | Load Mode Register |
| iSBX 0 | $FD0300 | Select 0 | Select 0 |
| | $FD0400 | Select 1 | Select 1 |
| iSBX 1 | $FD0500 | Select 0 | Select 0 |
| | $FD0600 | Select 1 | Select 1 |
| LEDs | $FD0800 | Invalid | Load register |

## 4-3 LED Programming

Eight status LEDs (red light-emitting diodes) are mounted along the top edge of the M68K10 to the right of the J1 header. An 8-bit write-only register addressed at $FD0800 is used to control these indicators. Bit 0 (the least significant bit) controls the right-most LED (the one next to the green LED). Bit 1 controls the second from the right, etc. Setting a bit to 0 will cause its LED to be illuminated; setting a bit to 1 will cause the LED to be dark.

## 4-4 Power-Up And Reset Programming

At power-up, and whenever a Reset is issued to the M68K10, the 68000 reads the supervisor stack pointer and program counter from the first eight bytes of the PROMs installed in sockets U16 and U17. The PROBUG PROMs installed in sockets U16 and U17 provide the necessary eight bytes for the 68000 to use at power-up.

## 4-5 I/O Programming Examples

The following pages contain listings of I/O programming examples. Use these examples to supplement the programming information supplied in the I/O devices' data books.

# 5. SUPPORT INFORMATION

This section contains pin assignments for the MULTIBUS P1 and P2 connectors, the iSBX connectors and the J1 and J2 I/O headers. In addition, it contains a parts list, schematics and the component identification silk screen.

## 5-1 J1 Serial I/O Header Pin Assignments

J1 is the 50-pin header on the left side of the top edge of the M68K10. The signals are arranged so that the M68K10 may be directly connected to a terminal and printer using 50-conductor flat cable, split into two 25-conductor cables and terminated with Winchester Electronics P.N. 49-1125P D-connectors or equivalent. To order such a cable from SBE, specify part number CBL-68K10.

Figure 5-1 identifies the signal on each pin of J1, and its corresponding RS-232C pin number. J1 pins 1-25 connect to one D-connector; pins 26-50 connect to the other. Pins which do not carry a signal show "N.C." (no connection) in the signal column.

Figure 5-1: J1 Serial I/O Header Pin Assignments

| J1 Pin # | Signal | RS-232 Pin # | J1 Pin # | Signal | RS-232 Pin # |
|---|---|---|---|---|---|
| 1 | GND | 1 | 2 | N.C. | 14 |
| 3 | Ch. B RXD | 2 | 4 | N.C. | 15 |
| 5 | Ch. B TXD | 3 | 6 | N.C. | 16 |
| 7 | N.C. | 4 | 8 | N.C. | 17 |
| 9 | N.C. | 5 | 10 | N.C. | 18 |
| 11 | N.C. | 6 | 12 | N.C. | 19 |
| 13 | GND | 7 | 14 | N.C. | 20 |
| 15 | N.C. | 8 | 16 | N.C. | 21 |
| 17 | N.C. | 9 | 18 | N.C. | 22 |
| 19 | N.C. | 10 | 20 | N.C. | 23 |
| 21 | N.C. | 11 | 22 | N.C. | 24 |
| 23 | N.C. | 12 | 24 | N.C. | 25 |
| 25 | N.C. | 13 | 26 | GND | 1 |
| 27 | N.C. | 14 | 28 | Ch. A RXD | 2 |
| 29 | N.C. | 15 | 30 | Ch. A TXD | 3 |
| 31 | N.C. | 16 | 32 | Ch. A CTS | 4 |
| 33 | N.C. | 17 | 34 | Ch. A RTS | 5 |
| 35 | N.C. | 18 | 36 | Ch. A DTR | 6 |
| 37 | N.C. | 19 | 38 | GND | 7 |
| 39 | Ch. A CD | 20 | 40 | Ch. A RTS | 8 |
| 41 | N.C. | 21 | 42 | N.C. | 9 |
| 43 | N.C. | 22 | 44 | N.C. | 10 |
| 45 | N.C. | 23 | 46 | N.C. | 11 |
| 47 | N.C. | 24 | 48 | N.C. | 12 |
| 49 | N.C. | 25 | 50 | N.C. | 13 |

## 5-2 J2 I/O Header Pin Assignments

J2 is located on the right side of the top edge of the M68K10. Figure 5-2 identifies the signal on each pin of J2.

Figure 5-2: J2 I/O Header Pin Assignments

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | GND | 2 | PB7 |
| 3 | GND | 4 | PB6 |
| 5 | GND | 6 | PB5 |
| 7 | GND | 8 | PB4 |
| 9 | GND | 10 | PB3 |
| 11 | GND | 12 | PB2 |
| 13 | GND | 14 | PB1 |
| 15 | GND | 16 | PB0 |
| 17 | GND | 18 | PC3 |
| 19 | GND | 20 | PC2 |
| 21 | GND | 22 | PC1 |
| 23 | GND | 24 | PC0 |
| 25 | GND | 26 | PC4 |
| 27 | GND | 28 | PC5 |
| 29 | GND | 30 | * |
| 31 | GND | 32 | * |
| 33 | GND | 34 | PA7 |
| 35 | GND | 36 | PA6 |
| 37 | GND | 38 | PA5 |
| 39 | GND | 40 | PA4 |
| 41 | GND | 42 | PA3 |
| 43 | GND | 44 | PA2 |
| 45 | GND | 46 | PA1 |
| 47 | GND | 48 | PA0 |
| 49 | GND | 50 | Ext. Interrupt |

* The signals on pin 30 and 32 of J2 are selected by jumpers at jumper areas J34 and J35. See section 3-7.

## 5-3 Battery Backup Connector Pin Assignments

Figure 5-3:
Pin Assignments Of Connector J40

| Pin # | Signal |
|---|---|
| 1 | Ground |
| 2 | +5V to CMOS RAM |
| 3 | PRO memory write protect |

## 5-4 Reset Connector Pin Assignments

Figure 5-4:
Pin Assignments Of Connector J3

| Pin # | Function |
|---|---|
| 1 | Ground for Reset switch |
| 2 | Reset switch normally open |

## 5-5 iSBX Connectors J31 and J33

Figure 5-5: Pin Assignments For iSBX Connectors, J31 & J33

| Pin | Mnemonic | Description | Pin | Mnemonic | Description |
|---|---|---|---|---|---|
| 35 | GND | SIGNAL GROUND | 36 | +5V | +5 Volts |
| 33 | MD0 | MDATA BIT 0 | 34 | — | RESERVED |
| 31 | MD1 | MDATA BIT 1 | 32 | — | RESERVED |
| 29 | MD2 | MDATA BIT 2 | 30 | OPT0 | OPTION 0 |
| 27 | MD3 | MDATA BIT 3 | 28 | OPT1 | OPTION 1 |
| 25 | MD4 | MDATA BIT 4 | 26 | — | RESERVED |
| 23 | MD5 | MDATA BIT 5 | 24 | — | RESERVED |
| 21 | MD6 | MDATA BIT 6 | 22 | MCS0/ | M CHIP SELECT 0 |
| 19 | MD7 | MDATA BIT 7 | 20 | MCS1/ | M CHIP SELECT 1 |
| 17 | GND | SIGNAL GROUND | 18 | +5V | +5 Volts |
| 15 | IORD/ | IO READ COMMAND | 16 | MWAIT/ | M WAIT |
| 13 | IOWRT/ | IO WRITE COMMAND | 14 | MINTR0 | M INTERRUPT 0 |
| 11 | MA0 | M ADDRESS 0 | 12 | MINTR1 | M INTERRUPT 1 |
| 9 | MA1 | M ADDRESS 1 | 10 | — | RESERVED |
| 7 | MA2 | M ADDRESS 2 | 8 | MPST/ | M PRESENT |
| 5 | MRESET | M RESET | 6 | MCLK | M CLOCK |
| 3 | GND | SIGNAL GROUND | 4 | +5V | +5 Volts |
| 1 | +12V | +12 Volts | 2 | -12V | -12 Volts |

### 5-5-1 User-Defined MULTIMODULE Options

Jumper areas J30 and J32 allow you to use two pins from each of the two iSBX connectors for user-defined options on MULTIMODULE boards. J30 corresponds to pins 28 and 30 of the J31 connector; J32 corresponds to pins 28 and 30 of the J33 connector.

Alternatively, you can use J30 and J32 to route signals from the M68K10 to the iSBX connectors.

## 5-6 MULTIBUS P1 and P2 Edge Connector Pin Assignments

Figures 5-6a and 5-6b on the following pages list the pin assignments of the Mulitbus P1 and P2 connectors. Only four signals are connected to the P2 connector; they are shown in Figure 5-6b. All other pins of P2 are N.C. (not connected).

Figure 5-6a: MULTIBUS P1 Pin Assignments

| | | (COMPONENT SIDE) | | | (CIRCUIT SIDE) | |
|---|---|---|---|---|---|---|
| | PIN[1] | MNEMONIC | DESCRIPTION | PIN[1] | MNEMONIC | DESCRIPTION |
| POWER SUPPLIES | 1 | GND | Signal GND | 2 | GND | Signal GND |
| | 3 | +5V | +5Vdc | 4 | +5V | +5Vdc |
| | 5 | +5V | +5Vdc | 6 | +5V | +5Vdc |
| | 7 | +12V | +12Vdc | 8 | +12V | +12Vdc |
| | 9 | -5V | -5Vdc | 10 | -5V | -5Vdc |
| | 11 | GND | Signal GND | 12 | GND | Signal GND |
| BUS CONTROLS | 13 | BCLK/ | Bus Clock | 14 | INIT/ | Initialize |
| | 15 | BPRN/ | Bus Priority In | 16 | BPRO/ | Bus Priority Out |
| | 17 | BUSY/ | Bus Busy | 18 | BREQ/ | Bus Request |
| | 19 | MRDC/ | Mem Read Cmd | 20 | MWTC/ | Mem Write Cmd |
| | 21 | IORC/ | I/O Read Cmd | 22 | IOWC/ | I/O Write Cmd |
| | 23 | XACK/ | XFER Acknowledge | 24 | INH1/ | Inhibit RAM[2] |
| BUS CONTROLS AND ADDRESS | 25 | — | Reserved | 26 | INH2/ | Inhibit ROM[2] |
| | 27 | BHEN/ | Byte High Enable | 28 | AD10/ | |
| | 29 | CBRQ/ | Common Bus Request | 30 | AD11/ | Address |
| | 31 | CCLK/ | Constant Clk | 32 | AD12/ | Bus |
| | 33 | — | Reserved | 34 | AD13/ | |
| INTERRUPTS | 35 | INT6/ | Parallel | 36 | INT7/ | Parallel |
| | 37 | INT4/ | Interrupt | 38 | INT5/ | Interrupt |
| | 39 | INT2/ | Requests | 40 | INT3/ | Requests |
| | 41 | INT0/ | | 42 | INT1/ | |
| ADDRESS | 43 | ADRE/ | | 44 | ADRF/ | |
| | 45 | ADRC/ | | 46 | ADRD/ | |
| | 47 | ADRA/ | Address | 48 | ADRB/ | Address |
| | 49 | ADR8/ | Bus | 50 | ADR9/ | Bus |
| | 51 | ADR6/ | | 52 | ADR7/ | |
| | 53 | ADR4/ | | 54 | ADR5/ | |
| | 55 | ADR2/ | | 56 | ADR3/ | |
| | 57 | ADR0/ | | 58 | ADR1/ | |
| DATA | 59 | DATE/ | | 60 | DATF/ | |
| | 61 | DATC/ | | 62 | DATD/ | |
| | 63 | DATA/ | | 64 | DATB/ | |
| | 65 | DAT8/ | Data | 66 | DAT9/ | Data |
| | 67 | DAT6/ | Bus | 68 | DAT7/ | Bus |
| | 69 | DAT4/ | | 70 | DAT5/ | |
| | 71 | DAT2/ | | 72 | DAT3/ | |
| | 73 | DAT0/ | | 74 | DAT1/ | |
| POWER SUPPLIES | 75 | GND | Signal GND | 76 | GND | Signal GND |
| | 77 | — | Reserved | 78 | — | Reserved |
| | 79 | -12V | -12Vdc | 80 | -12V | -12Vdc |
| | 81 | +5V | +5Vdc | 82 | +5V | +5Vdc |
| | 83 | +5V | +5Vdc | 84 | +5V | +5Vdc |
| | 85 | GND | Signal GND | 86 | GND | Signal GND |

1. All odd-numbered pins (1, 3, 5 . . . 85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

Figure 5-6b: MULTIBUS P2
Pin Assignments

| Pin # | Signal |
|---|---|
| 55 | ADR16/ |
| 56 | ADR17/ |
| 57 | ADR14/ |
| 58 | ADR15/ |

**5-7 Parts List, Silk Screen and Schematics**

The following pages contain additional reference data for the M68K10.

## M68K10 Parts List

The following table lists integrated circuit components and sockets on the ModulasTen M68K10. The SBE part number is given for reference; equivalent parts from other manufacturers may be used depending on supply.

| On-Board Identification | SBE Part# | Description |
|---|---|---|
| BYPASS | 43149 | Capacitor, .022mfd, 50V |
| C1 C3 | 43167 | Capacitor, Tant., 33uF, 20V |
| C2 C4 | 43166 | Capacitor, Tant., 100uF, 10V |
| C9-C12 | 43163 | Capacitor, 39uF, 10V |
| D1 D2 | 44691 | LED QUAD Logic, Red |
| D3 | 44690 | LED, Logic State, Green |
| J1 J2 | 21517 | Header, D.R., Rt-Angle, M, 50 Cond. [3M] |
| J20 J31 J33 | 21302 | Header, iSBX, D.R., F, 36 Cond. |
| Q1 | 45225 | Transistor, 2N2222A, Switch, NPN, 40V |
| R1 R2 R3 R12 R13 | 41076 | Resistor, 750 1/4W 5% |
| R4 | 41055 | Resistor, 33 1/4W 5% |
| R5 R6 R7 R11 | 41103 | Resistor, 10K 1/4W 5% |
| R9 | 41115 | Resistor, 33K 1/4W 5% |
| R10 | 41128 | Resistor, 100K 1/4W 5% |
| RP1 RP2 RP4 | 41668 | Resistor Net., 3.3K 10-pin, SIP |
| RP3 | 41667 | Resistor Net., 1.0K 8-pin, SIP |
| RP5 RP6 RP7 | 41660 | Resistor Net., 33 8-pin, SIP |
| S1 | 30102 | Switch, Momentary Pushbutton |
| U1 | 54382 | 1488 Quad Line Driver |
| U2 | 54383 | 1489 Quad Line Receiver |
| U3 U61 U85 U86 | 51141 | 74LS245 Buffer, Tri-state, Octal |
| U4 U31 U45 U69 | 51148 | 74LS273 Octal D-type, Flip-Flop |
| U6 | 55508 | 8255A-5, Hi-Speed Parallel I/O |
| U7 | 55505-5 | 8253-5, Hi-Speed Triple Timer |
| U8 | 55509 | 556 Dual Timer, |
| U9 | 51125 | 74LS175 Register, D-type Quad |
| U10 | 55513 | 8116 Dual Baud Rate Generator, 5V |
| U11 | 48992 | Crystal, 20 MHz, DIP |
| U12 | 51080 | 74LS74 Dual D Flip-Flop |
| U13 | 55510 | P51 8274 Serial Controller, 3MHz, Plastic |
| U14 U33 | 51067 | 74LS30 8-Input NAND |
| U15 | 50007 | 7407 HEX Buffer, O.C. |
| U18 U19 U40 U43 U44 | 56380 | PAL, 16L8, Plastic |
| U20 | 51096 | 74LS138 3-to-8 Decoder |
| U21 U30 | 55511 | Delay Line, 125nS, w/ 25nS Taps |
| U22 U29 U37 | 52300 | 74S00 Quad, 2-Input NAND |
| U23 | 51068 | 74LS32 Quad, 2-Input OR |
| U24 | 51058 | 74LS10 Triple 3-Input NAND |
| U25 | 52313 | 74S175 Register, Quad D-Type |
| U26 | 51090 | 74LS123 Dual One-Shot |
| U27 | - | not used |
| U28 | 56381 | PAL, 16R8, Plastic |

M68K10 Parts List (Continued)

| | | |
|---|---|---|
| U29 | | see U22 |
| U30 | | see U21 |
| U31 | | see U4 |
| U32 | 52328 | 74S260, Dual 5-Input NOR |
| U33 | | see U14 |
| U34 U41 | 52301 | 74S02 Quad 2-Input NOR |
| U36 U46 | 51185 | 74LS393 Dual 4-Bit Binary Counter |
| U37 | | see U22 |
| U38 | 52315 | 74S51, Dual 4-Input And-Or-Invert |
| U39 | 52303 | 74S04 Hex Inverter |
| U40 | | see U18 |
| U41 | | see U34 |
| U42 | 51054 | 74LS04 Hex Inverter |
| U43 U44 | | see U18 |
| U45 | | see U4 |
| U46 | | see U36 |
| U47 U66 U68 U71, | 51189 | 74LS640, Octal Bus Trans., Inverting, 24mA |
| U72 U75 U76 | " | " |
| U48 | 55457 | 68000 MPU, 10 MHz |
| U49 U73 | 51105 | 74LS157 Quad 2-to-1 Multiplexer |
| U50 U74 | 52329 | 74S258, Quad 2-Input Multiplexer |
| U51-U58, U77-U84 | 56135-3 | 4164 RAM, 64K Dynamic, 150nS |
| U59 | - | not used |
| U60 | 52317 | 74S38, Quad 2-Input NAND, O.C. |
| U61 | | see U3 |
| U62 | 51192 | 74LS645-1, Octal Bus Trans., 48mA |
| U63 | 51095 | 74LS132 Quad 2-Input NAND, Schmitt |
| U64 | 52318 | 74S140, Dual 4-Input NAND, Line Driver |
| U65 | 53406 | 25LS2521 Comparator, 8-Bit |
| U66 | | see U47 |
| U67 | 51055 | 74LS05 Hex Inverter, O.C. |
| U68 | | see U47 |
| U69 | | see U4 |
| U70 | 51098 | 74LS148 Priority Encoder |
| U71 U72 | | see U47 |
| U73 | | see U49 |
| U74 | | see U50 |
| U75 U76 | | see U47 |
| U77-U84 | | see U51 |
| U85 U86 | | see U3 |
| Y1 | 48981 | Crystal, 5.0688 MHz, Series |

Codes For On-Board Identification

| | | | |
|---|---|---|---|
| C | Capacitor | R | Resistor |
| D | Diode (LED) | RP | Resistor Pack |
| J | Jumpers | S | Switch |
| Q | Transistor | U | Socket |
| | | Y | Crystal |

```
                 00000064 LEVEL1  EQU     $64             LEVEL 1 interrupt autovector
                 00000068 LEVEL2  EQU     $68             LEVEL 2 interrupt autovector

                 00FD0000 MPSC    EQU     $FD0000         Address of NEC 7201 (8274)
                 00FD0000 MPSCA   EQU     MPSC            Address of CHANNEL A
                 00FD0002 MPSCB   EQU     MPSC+2          Address of CHANNEL B
                 00000004 STATUS  EQU     4               Offset to MPSC status port
                 00000004 CMD     EQU     4               Offset of MPSC command port
                 00000000 INPUT   EQU     0               RX status bit
                 00000002 OUTPUT  EQU     2               TX status bit

                 00FD0100 PPI     EQU     $FD0100         Address of 8255 PPI
                 00000000 PORTA   EQU     0               Port A
                 00000002 PORTB   EQU     2               Port B
                 00000004 PORTC   EQU     4               Port C
                 00000006 PPICONTROL EQU  6               PPI control word

                 00FD0200 TIMER   EQU     $FD0200         Address of 8253 interval timer
                 00000000 TIMER0  EQU     0               Timer 0
                 00000002 TIMER1  EQU     2               Timer 1
                 00000004 TIMER2  EQU     4               Timer 2
                 00000006 TIMERCONTROL EQU 6              Timer control word

001000                            ORG     $1000
001000 0000 0000          TICKS   DC.L    0               Real time clock
001004 0000 0000          COUNT   DC.L    0               Count down clock
001008 00                 CHAINT  DC.B    0               CHANNEL A interrupts active fl
001009 00                 CHBINT  DC.B    0               CHANNEL B interrupts active fl
00100A 00                 ACKFLAG DC.B    0               MULTIBUS acknowledge flag

002000                            ORG     $2000

                          **      INI - INITIALIZE MPSC
                          *
                          *       INI initializes both channels of the MPSC using
                          *       a table of MPSC register numbers and values.
                          *       By selecting the desired table, an MPSC channel may
                          *       by set up for non-interrupt I/O or interrupts on
                          *       input, output, or both.
                          *

002000 41F9 0000 2026     INI     LEA     INIA,A0         CHANNEL A set up options
002006 43F9 0000 2026             LEA     INIA,A1         CHANNEL B set up options
00200C 45F9 00FD 0004             LEA     MPSC+STATUS,A2  CHANNEL A control register
002012 1012                       MOVE.B  (A2),D0         Synchronize MPSC register acce
002014 102A 0002                  MOVE.B  2(A2),D0
002018 7008                       MOVE.L  #8,D0           Length of initialization array

00201A 1498               INI1    MOVE.B  (A0)+,(A2)      CHANNEL A
00201C 1559 0002                  MOVE.B  (A1)+,2(A2)     CHANNEL B
002020 51C8 FFF8}00201A           DBRA    D0,INI1
002024 4E75                       RTS
```

```
                 00002026  INIA    EQU      *           Non-interrupt initialization
  002026 18                        DC.B     $18         Reset channel
  002027 044C                      DC.B     $04,$4C     Asynchronous mode, /16 clock,
                           *                            2 stop bits, no parity
  002029 03E1                      DC.B     $03,$E1     8-BIT RX character, auto enabl
                           *                            Input enable
  00202B 05EA                      DC.B     $05,$EA     DTR on, 8-BIT TX character,
                           *                            XMIT enable, RTS on
  00202D 0000                      DC.B     $00,$00     Dummies not used in this mode

                 0000202F  INIB    EQU      *           Input interrupt initialization
  00202F 18                        DC.B     $18         Reset channel
  002030 044C                      DC.B     $04,$4C     Asynchronous mode, /16 clock,
                           *                            2 stop bits, no parity
  002032 03E1                      DC.B     $03,$E1     8-BIT RX character, auto enabl
                           *                            Input enable
  002034 05EA                      DC.B     $05,$EA     DTR on, 8-BIT TX character,
                           *                            XMIT enable, RTS on
  002036 0118                      DC.B     $01,$18     Input interrupts on, no INT ve

                 00002038  INIC    EQU      *           Input and output interrupts
  002038 18                        DC.B     $18         Reset channel
  002039 044C                      DC.B     $04,$4C     Asynchronous mode, /16 clock,
                           *                            2 stop bits, no parity
  00203B 03E1                      DC.B     $03,$E1     8-BIT RX character, auto enabl
                           *                            Input enable
  00203D 05EA                      DC.B     $05,$EA     DTR on, 8-BIT TX character,
                           *                            XMIT enable, RTS on
  00203F 011A                      DC.B     $01,$1A     Input/output interrupts on

                 00002041  INID    EQU      *           Vectored interrupt initializat
  002041 18                        DC.B     $18         Reset channel
  002042 044C                      DC.B     $04,$4C     Asynchronous mode, /16 clock,
                           *                            2 stop bits, no parity
  002044 03E1                      DC.B     $03,$E1     8-BIT RX character, auto enabl
                           *                            Input enable
  002046 05EA                      DC.B     $05,$EA     DTR on, 8-BIT TX character,
                           *                            XMIT enable, RTS on
  002048 011E                      DC.B     $01,$1E     Interrupts on, INT vector set
```

```
                            **      RCA - READ CHARACTER FROM CHANNEL A
                            *
                            *       This routine assumes the MPSC character I/O
                            *       is not interrupt-driven.  The status port
                            *       of the MPSC is polled until a character is
                            *       available.
                            *
                            *       EXIT  (D0) = CHARACTER READ FROM MPSC
                            *

00204A 0839 0000 00FD   RCA      BTST     #INPUT,MPSCA+STATUS Wait on character received
002052 67F6      }00204A         BEQ      RCA
002054 1039 00FD 0000            MOVE.B   MPSCA,D0          Read character
00205A 0240 007F                 AND.W    #$7F,D0           Ignore parity
                            *
                            *       Drop through to echo the character
                            *



                            **      WCA - WRITE CHARACTER TO CHANNEL A
                            *
                            *       This routine assumes the MPSC character I/O
                            *       is not interrupt-driven.  The status port
                            *       of the MPSC is polled until the transmit
                            *       port will accept the next character.
                            *
                            *       ENTRY (D0) = CHARACTER TO WRITE
                            *

00205E 0839 0002 00FD   WCA      BTST     #OUTPUT,MPSCA+STATUS Wait on transmitter empty
002066 67F6      }00205E         BEQ      WCA
002068 13C0 00FD 0000            MOVE.B   D0,MPSCA          Output character
00206E 4E75                      RTS
```

```
                       **      MPSCINT - MPSC INTERRUPT PROCESSING
                       *
                       *       This interrupt routine inspects the status
                       *       registers of both channels and handles any
                       *       input or output interrupt.  If no more characters
                       *       are available for output on an output interrupt,
                       *       the output interrupts are turned off.  They are
                       *       automatically started again when a character is
                       *       output to the appropriate port by the background
                       *       program.  An output-interrupts-active flag must be
                       *       maintained to avoid output conflicts.
                       *

002070 48E7 8000       MPSCINT MOVEM.L  D0,-(A7)        Save registers
002074 0839 0000 00FD          BTST     #INPUT,MPSCA+STATUS
00207C 6706     }002084        BEQ.S    MPSCI1          Jump if no CHANNEL A input interrup
00207E 1039 00FD 0000          MOVE.B   MPSCA,D0
                       *         .
                       *         .                      Put byte in buffer, ETC
                       *         .
002084 0839 0000 00FD  MPSCI1  BTST     #INPUT,MPSCB+STATUS
00208C 6706     }002094        BEQ.S    MPSCI2          Jump if no CHANNEL B input interrup
00208E 1039 00FD 0002          MOVE.B   MPSCB,D0
                       *         .
                       *         .                      Put byte in buffer, ETC
                       *         .
002094 0839 0002 00FD  MPSCI2  BTST     #OUTPUT,MPSCA+STATUS
00209C 6714     }0020B2        BEQ.S    MPSCI3          Jump if no CHANNEL A output interru
                       *         .
                       *         .                      Get CHANNEL A next output byte
                       *         .
00209E 13C0 00FD 0000          MOVE.B   D0,MPSCA        Output byte
0020A4 600C     }0020B2        BRA.S    MPSCI3
                       *
                       *                                If no more CHANNEL A output
0020A6 13FC 0028 00FD          MOVE.B   #$28,MPSCA+CMD  Turn off OUTPUT interrupts
0020AE 4238 1008               CLR.B    CHAINT          Flag CHANNEL A interrupts off
                       *
0020B2 0839 0002 00FD  MPSCI3  BTST     #OUTPUT,MPSCB+STATUS
0020BA 6714     }0020D0        BEQ.S    MPSCI4          Jump if no CHANNEL B OUTPUT interru
                       *         .
                       *         .                      Get CHANNEL B next output byte
                       *         .
0020BC 13C0 00FD 0002          MOVE.B   D0,MPSCB        Output byte
0020C2 600C     }0020D0        BRA.S    MPSCI4
                       *
                       *                                If no more CHANNEL B output
0020C4 13FC 0028 00FD          MOVE.B   #$28,MPSCB+CMD  Turn off OUTPUT interrupts
0020CC 4238 1009               CLR.B    CHBINT          Flag CHANNEL B interrupts off
                       *
0020D0 4CDF 0001       MPSCI4  MOVEM.L  (A7)+,D0        Restore registers
0020D4 4E73                    RTE
```

```
                        **      OUTCHA - OUTPUT TO CHANNEL A
                        *
                        *       This is the character output routine that sets up
                        *       the output buffer for the interrupt routine (MPSCINT).
                        *       The MPSC only interrupts after a character has
                        *       been output, so the first character has to be
                        *       handled from outside the interrupt routine.
                        *
                        *       The first character is output and CHAINT is set.
                        *       Thereafter, characters are buffered (to be output
                        *       by MPSCINT).  When MPSCINT empties the buffer it clears
                        *       CHAINT.
                        *
                        *       ENTRY (D0) = BYTE TO OUTPUT
                        *

 0020D6 40E7            OUTCHA  MOVE     SR,-(A7)         Save interrupt level
 0020D8 007C 0700               OR       #$700,SR         Turn interrupts off
 0020DC 4A38 1008               TST.B    CHAINT
 0020E0 6610    }0020F2         BNE.S    OUTCHA1          Jump if MPSC interrupts already

 0020E2 11FC 0001 1008          MOVE.B   #1,CHAINT        Flag interrupts active
 0020E8 13C0 00FD 0000          MOVE.B   D0,MPSCA         Output byte
 0020EE 46DF                    MOVE     (A7)+,SR         Restore interrupts
 0020F0 4E75                    RTS

              000020F2  OUTCHA1 EQU      *
                        *        .
                        *        .         Put character in buffer
                        *        .
 0020F2 46DF                    MOVE     (A7)+,SR         Restore interrupts
 0020F4 4E75                    RTS
```

```
                              **      TIMERSETUP - TIMER SETUP ROUTINE
                              *
                              *       This the initialization routine for the timer
                              *       interrupt routine (TIMERINT).
                              *       Since the timer can start interrupting before
                              *       it is configured properly, it must be setup
                              *       before the interrupts are enabled.
                              *
                              *
                              *       The M68K10 board is assumed to be configured
                              *       as follows:
                              *
                              *       JUMPER J8
                              *         A2-B2     78.125 KHz clock rate
                              *
                              *       JUMPER J34
                              *         A1-B1     Connect clock rate to timer 0
                              *
                              *       JUMPER J29
                              *         A6-B6     On-board interrupt from timer 0
                              *
                              *       JUMPER J6
                              *         A2-B2     Interrupt from timer 0 to LEVEL 2 interrupt
                              *

                 000020F6   TIMERSETUP EQU   *
 0020F6 41F9 0000 211C              LEA      TIMERINT,A0
 0020FC 21C8 0068                   MOVE.L   A0,LEVEL2        Initialize exception vector

 002100 41F9 00FD 0200              LEA      TIMER,A0
 002106 117C 0030 0006              MOVE.B   #$30,TIMERCONTROL(A0) Timer 0; 16 bits, mode 0
 00210C 303C 030A                   MOVE.W   #778,D0          Initial count
 002110 1080                        MOVE.B   D0,(A0)
 002112 E048                        LSR.W    #8,D0
 002114 1080                        MOVE.B   D0,(A0)
 002116 027C F8FF                   AND      #$F8FF,SR        Enable interrupts
 00211A 4E75                        RTS
```

```
                              **      TIMERINT - TIMER INTERRUPT ROUTINE
                              *
                              *       Timer 0 interrupts every 1/100th of a second.
                              *       While the interrupt is pending the timer
                              *       continues counting down.  The interrupt routine
                              *       adds this negative amount to the next interval
                              *       count to reduce the cumulative error in the timer
                              *       value.
                              *
                              *       This interrupt routine updates two timers, TICKS and
                              *       COUNT.  TICKS advances continuously every 1/100th of
                              *       a second.  COUNT counts down to zero and then stops
                              *       counting.
                              *
                    0000211C  TIMERINT EQU     *
 00211C 48E7 8080                     MOVEM.L  D0/A0,-(A7)
 002120 41F9 00FD 0200                LEA      TIMER,A0
 002126 007C 0700                     OR       #$0700,SR       Disable higher priority interrup
 00212A 117C 0000 0006                MOVE.B   #0,TIMERCONTROL(A0) Latch timer value
 002130 1010                          MOVE.B   (A0),D0         Get low byte
 002132 E148                          LSL.W    #8,D0
 002134 1010                          MOVE.B   (A0),D0         Get high byte
 002136 E158                          ROL.W    #8,D0           Exchange low and high bytes
 002138 0640 030A                     ADD.W    #778,D0         Add in next interval count
 00213C 1080                          MOVE.B   D0,(A0)         Set new count
 00213E E048                          LSR.W    #8,D0
 002140 1080                          MOVE.B   D0,(A0)

 002142 52B8 1000                     ADD.L    #1,TICKS        Advance real-time clock
 002146 4AB8 1004                     TST.L    COUNT
 00214A 6704     }002150              BEQ.S    TIMRI2
 00214C 53B8 1004                     SUB.L    #1,COUNT        Decrement count down timer
 002150 4CDF 0101             TIMRI2  MOVEM.L  (A7)+,D0/A0
 002154 4E73                          RTE
```

```
                        **      INITPRINT - INITIALIZE PRINTER PORT
                        *
                        *       The parallel printer interface board (PTR-1E)
                        *       allows a Centronix-type printer to be controlled
                        *       through the 8255 parallel port.
                        *
                        *       The printer control lines are connected to
                        *       the B port of the PPI.  They are defined as
                        *       follows:
                        *         1    Printer select
                        *         2    Auto linefeed
                        *         4    Initialize printer
                        *         8    Enable interrupt on error
                        *
                        *       The printer status lines are connected to
                        *       the C port as follows:
                        *         1    Paper out
                        *         2    Printer error
                        *         4    Printer busy
                        *        10    Printer selected
                        *
                        *       The character to be printed is output to
                        *       the A port.
                        *
                        *
                        *       The M68K10 board is assumed to be configured
                        *       as follows:
                        *
                        *       JUMPER J34
                        *         A4-B4     PC7 connected to pin 32 of J2
                        *
                        *       JUMPER J35
                        *         A4-A4     PC6 connected to pin 30 of J2
                        *
             00002156   INITPRINT EQU    *
 002156 41F9 00FD 0100          LEA      PPI,A0
 00215C 117C 00A9 0006          MOVE.B   #$A9,PPICONTROL(A0) Port A is output, mode 1
                        *                                    Port B is output, mode 0
                        *                                    Port C is input
 002162 117C 0005 0002          MOVE.B   #5,PORTB(A0)    Initialize printer

 002168 303C 2710               MOVE.W   #10000,D0       Pause at least 100 microseconds
 00216C 51C8 FFFE}00216C        DBRA     D0,*

 002170 117C 0001 0002          MOVE.B   #1,PORTB(A0)    Select printer
 002176 4E75                    RTS
```

```
                         **      PRINT - PARALLEL PRINTER DRIVER
                         *
                         *       ENTRY (D0) = CHARACTER TO BE PRINTED
                         *
                         *       This routine waits for any errors or
                         *       not ready conditions to be cleared.
                         *

 002178 48E7 4080        PRINT   MOVEM.L  D1/A0,-(A7)
 00217C 41F9 00FD 0100           LEA      PPI,A0            Base address of parallel port
 002182 1228 0004        PRINT2  MOVE.B   PORTC(A0),D1
 002186 0201 0007                AND.B    #$07,D1
 00218A 66F6      }002182        BNE      PRINT2            Wait until printer ready
 00218C 1140 0000                MOVE.B   D0,PORTA(A0)      Output character to printer
 002190 4CDF 0102                MOVEM.L  (A7)+,D1/A0
 002194 4E75                     RTS


                         **      BAUD - PROGRAMMABLE BAUD RATE
                         *
                         *       The M68K10 board can be jumpered to use the
                         *       output of timer 2 as the baud rate to either
                         *       of the serial ports.
                         *
                         *       ENTRY (D0) = Desired baud rate
                         *                    For example 300, 1200, 9600
                         *
                         *       The M68K10 board is assumed to be configured
                         *       as follows:
                         *
                         *       JUMPER J8
                         *         A1-B1     1.250 MHz clock rate
                         *
                         *       JUMPER J28
                         *         A1-A2     Programmable baud rate for channel A
                         *

 002196 41F9 00FD 0200   BAUD    LEA      TIMER,A0
 00219C 117C 00B6 0006           MOVE.B   #$B6,TIMERCONTROL(A0) Timer 2; 16 bits, square

 0021A2 223C 0001 312D           MOVE.L   #1250000/16,D1    Source clock rate/16
 0021A8 82C0                     DIVU     D0,D1             Calculate timer interval
 0021AA 1141 0004                MOVE.B   D1,TIMER2(A0)     Set timer value
 0021AE E059                     ROR.W    #8,D1
 0021B0 1141 0004                MOVE.B   D1,TIMER2(A0)
 0021B4 4E75                     RTS
```

```
                      **      MULTI - GENERATING MULTIBUS INTERRUPTS
                      *
                      *       PC3 of the 8255 PPI can be jumpered to generate
                      *       interrupts on the MULTIBUS.
                      *
                      *       This routine generates INT1 on the MULTIBUS.
                      *       The board receiving the interrupt clears
                      *       ACKFLAG in shared memory to indicate that
                      *       the interrupt has been received.
                      *
                      *
                      *       The M68K10 board is assumed to be configured
                      *       as follows:
                      *
                      *       JUMPER J29
                      *         A8-B8     Interrupt from PC3 of PPI
                      *
                      *       JUMPER J6
                      *         B5-C5     Interrupt from PC3 to MULTIBUS INT1
                      *

 0021B6 41F9 00FD 0100   MULTI   LEA      PPI,A0           Base address of PPI
 0021BC 117C 009A 0006           MOVE.B   #$9A,PPICONTROL(A0) Port C (lower) output

 0021C2 11FC 00FF 100A           MOVE.B   #$FF,ACKFLAG     Set interrupt acknowledge flag
 0021C8 117C 0008 0004           MOVE.B   #$08,PORTC(A0)   Generate interrupt

 0021CE 4A38 100A        MULTI2  TST.B    ACKFLAG
 0021D2 66FA     }0021CE         BNE      MULTI2           Wait for interrupt acknowledge

 0021D4 117C 0000 0004           MOVE.B   #$00,PORTC(A0)   Remove interrupt from MULTIBUS
 0021DA 4E75                     RTS


                                 END
0 ERROR(S) DETECTED
```